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(71) Applicant: SEMITOOL, INC. [US/US]; 655 West Reserve Drive, Kalispell, MT 59901 (US).

(72) Inventors: STEVENS, E., Henry; 18 Loma Linda Drive, Colorado Springs, CO 80906 (US). BERNER, Robert, W.; 2831 West Timber Drive, Eagle, ID 83616 (US).

(74) Agent: CHAPA, Lawrence, J.; Rockey, Milnamow & Katz, Two Prudential Plaza, 47th floor, 180 North Stetson Avenue, Chicago, IL 60601 (US).

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(54) Title: PROCESS AND MANUFACTURING TOOL ARCHITECTURE FOR USE IN THE MANUFACTURE OF ONE OR MORE METALLIZATION LEVELS ON A WORKPIECE

(57) Abstract

A semiconductor manufacturing tool configuration and corresponding process for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a semiconductor workpiece with a minimal number of workpiece transfer operations between the tool sets is disclosed.

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TITLE OF THE INVENTION

PROCESS AND MANUFACTURING TOOL ARCHITECTURE FOR USE IN THE MANUFACTURE OF ONE OR MORE METALLIZATION LEVELS ON A WORKPIECE

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

BACKGROUND OF THE INVENTION

An integrated circuit is an interconnected ensemble of devices formed within a semiconductor material and within a dielectric material that overlies a surface of the semiconductor material. Devices which may be formed within the semiconductor material include MOS transistors, bipolar transistors, diodes and diffused resistors. Devices which may be formed within the dielectric include thin-film resistors and capacitors. Typically, more than 100 integrated circuit die (IC chips) are constructed on a single 8 inch diameter silicon wafer. The devices utilized in each dice are interconnected by conductor paths formed within the dielectric. Typically, two or more levels of conductor paths, with successive levels separated by a dielectric layer, are employed as interconnections. In current practice, an aluminum alloy and silicon oxide are typically used for, respectively, the conductor and dielectric.

Delays in propagation of electrical signals between devices on a single

dice limit the performance of integrated circuits. More particularly, these delays limit the speed at which an integrated circuit may process these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

For each interconnect path, signal propagation delay may be characterized by a time delay τ. See E.H. Stevens, *Interconnect Technology*, QMC, Inc., July 1993. An approximate expression for the time delay, τ, as it relates to the transmission of a signal between transistors on an integrated circuit is given by the equation:

$$\tau = RC[\, 1 + (V_{SAT}/RI_{SAT})\,]$$

In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path, and I_{SAT} and V_{SAT} are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, ρ, of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K_e, of the dielectric material. A small value of τ requires that the interconnect line carry a current density sufficiently large to make the ratio V_{SAT}/RI_{SAT} small. It

follows, therefore, that a low-ρ conductor which can carry a high current density and a low-K_e dielectric should be utilized in the manufacture of high-performance integrated circuits.

To meet the foregoing criterion, copper interconnect lines within a low-K_e dielectric will likely replace aluminum-alloy lines within a silicon oxide dielectric as the most preferred interconnect structure. See "Copper Goes Mainstream: Low-k to Follow", *Semiconductor International*, November 1997, pp. 67-70. Resistivities of copper films are in the range of 1.7 to 2.0 μΩcm. while resistivities of aluminum-alloy films are higher in the range of 3.0 to 3.5 μΩcm.

Despite the advantageous properties of copper, several problems must be addressed for copper interconnects to become viable in large-scale manufacturing processes.

Diffusion of copper is one such problem. Under the influence of an electric field, and at only moderately elevated temperatures, copper moves rapidly through silicon oxide. It is believed that copper also moves rapidly through low-K_e dielectrics. Such copper diffusion causes failure of devices formed within the silicon.

Another problem is the propensity of copper to oxidize rapidly when immersed in aqueous solutions or when exposed an to oxygen-containing atmosphere. Oxidized surfaces of the copper are rendered non-conductive and thereby limit the current carrying capability of a given conductor path when

compared to a similarly dimensioned non-oxidized copper path.

A still further problem with using copper in integrated circuits is that it is difficult to use copper in a multi-layer, integrated circuit structure with dielectric materials. Using traditional methods of copper deposition, copper adheres only weakly to dielectric materials.

Finally, because copper does not form volatile halide compounds, direct plasma etching of copper cannot be employed in fine-line patterning of copper. As such, copper is difficult to use in the increasingly small geometries required for advanced integrated circuit devices.

The semiconductor industry has addressed some of the foregoing problems and has adopted a generally standard interconnect architecture for copper interconnects. To this end, the industry has found that fine-line patterning of copper can be accomplished by etching trenches and vias in a dielectric, filling the trenches and vias with a deposition of copper, and removing copper from above the top surface of the dielectric by chemical-mechanical polishing (CMP). An interconnect architecture called dual damascene can be employed to implement such an architecture and thereby form copper lines within a dielectric. Fig. 1 illustrates the process steps generally required for implementing the dual damascene architecture.

The present inventors have found that the dual damascene architecture may often be difficult for semiconductor manufacturers to implement in large-scale manufacturing processes. It is difficult to deposit a thin silicon nitride etch-

stop layer without damaging the underlying low K_e material. The art of plasma etching dielectric materials is well established, but etching sub-half-micrometer features in a low-K_e dielectric while maintaining selectivity to silicon nitride is difficult.

There are at least two processes in the formation of the dual-damascene architecture that are particularly troublesome. First, deposition of thin, uniform barrier and seed layers into high aspect ratio (depth/ diameter) vias and high aspect ratio (depth /width) trenches is difficult. The upper portions of such trenches and vias tend to pinch-off before the respective trench and/or via is completely filled or layered with the desired material. Further, CMP and the associated cleaning procedures are especially complex and difficult to implement.

In addition to its difficulty and complexity, the dual damascene architecture imposes limitations on interconnect performance. The etch-stop layer, typically comprised of silicon nitride, has a high dielectric permittivity; thus, unless the etch-stop layer is very thin compared to the line thickness, capacitance between metal lines in the same interconnect level is dominated by coupling through the etch stop. Conductivities of known barrier materials are negligible compared to the conductivity of copper; thus the conductance of narrow interconnect lines is markedly reduced by the barrier layer that must be interposed between the copper and dielectric.

A processing tool architecture suitable for implementing the dual-damascene process steps illustrated in Fig. 1 is shown in Fig. 2. As illustrated in

Fig. 2, the dual damascene architecture can be implemented with ten tool sets. Formation of each interconnect level generally requires two precision photolithographic processes, two precision etches, four dielectric depositions, barrier and seed layer depositions, a copper deposition, CMP and a post-CMP clean. Both small vias and small trenches must be etched; thus, an etch tool is required to define via features in the silicon nitride film, and a second etch tool is required to define via openings and trench features in the low-K_e dielectric. Using the traditional processing tool architecture of Fig. 2, the formation of each metallization level requires at least 13 workpiece movements among the tool sets.

The substantial number of wafer movements used to form a dual-damascene interconnect metallization structure reduces the reliability and yield of to manufacturing process. As the number of wafer movements increases, so does the potential for mis-handling of one or more wafers. Further, implementing a manufacturing facility for applying dual-damascene interconnect metallization structures requires a substantial capital outlay for above purchase of the required tool sets. Such reliability and capital equipment outlay issues are addressed by at least one aspect of the present invention.

In view of the foregoing problems, the present inventors have also recognized that copper metallization layers need an effective barrier material to prevent copper diffusion and an effective protective layer over the copper metallization to prevent oxidation of the copper. Existing processes for manufacturing such metallization layers are inefficient and are not economically

viable for use in large-scale manufacturing operations.

BRIEF SUMMARY OF THE INVENTION

A semiconductor manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a semiconductor workpiece with a minimal number of workpiece transfer operations between the tool sets is disclosed. The tool configuration comprises a film deposition tool set, a pattern processing tool set, a wet processing tool set, and a dielectric processing tool set. The film deposition tool set is used to deposit a conductive barrier layer exterior to the planar dielectric surface of the semiconductor workpiece and a conductive seed layer exterior to the barrier layer. The pattern processing tool set is used to provide an interconnect line pattern over the seed layer and to provide a post pattern over interconnect line metallization formed using the interconnect line pattern. The wet processing tool set is used to perform at least the following wet processing operations: applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed by the pattern processing tool set; removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern; and removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization. The dielectric processing tool set is used to deposit a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization.

A single metallization level may be formed using a plurality of workpiece movements between the tool sets. Preferably, no more than ten workpiece movements between the tool sets are used, and, even more preferably, no more than five workpiece movements between the tool sets are used.

In some instances, it may be necessary or desirable to use a hard mask for the patterning of the interconnect metallization. To this end, an alternative tool configuration comprises a film deposition tool set, a hard mask formation tool set, a hard mask etching tool set, a pattern processing tool set, a wet processing tool set, and a dielectric processing tool set. The film deposition tool set is used to deposit a conductive barrier layer exterior to the planar dielectric surface of the workpiece and a conductive seed layer exterior to the barrier layer. The hard mask formation tool set is used to form a hard mask dielectric layer exterior to the seed layer in accordance with one of the disclosed processes, and to form a still further hard mask dielectric layer exterior to the hard mask dielectric layer. In accordance with a first disclosed process, the pattern processing tool set is used to provide an interconnect line pattern over the hard mask dielectric layer and to provide a post pattern over interconnect line metallization formed using the interconnect line pattern. In accordance with a second disclosed process, the pattern processing tools set is used to provide a post pattern over the further hard mask dielectric layer so that the post pattern is ultimately formed in the further hard mask dielectric layer. The hard mask etching tool set is used to etch exposed regions of the hard mask dielectric layer after formation of the

interconnect line pattern thereover and, in accordance with the second disclosed process, the exposed portions of the further hard mask dielectric layer after the formation of the post pattern thereover. The wet processing tool set performs at least the following wet processing operations: 1) applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed by the pattern processing tool set, 2) removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern, 3) removing the hard mask dielectric layer and, if necessary, the further hard mask dielectric layer, and 4) removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization. The dielectric processing tool set is used to deposit a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization.

In accordance with a specific embodiment of the tool set architecture, an inspection tool set may also be included. The semiconductor workpieces are transferred to the inspection apparatus at various intermediate stages of the metallization process to insure, for example, proper registration of the pattern layers and resulting metallization structures. In such instances, a single metallization level may be formed using no more than ten workpiece movements between the tool sets. When using the hard mask tool architecture, it is preferable to use no more than fourteen workpiece movements between the tool sets are

used when an inspection tool set is employed. Even more preferably, no more than seven workpiece movements between the tool sets are used.

A process for providing one or more protected copper elements on a surface of a workpiece is also set forth. In accordance with the process, a barrier layer is applied to the workpiece. If the barrier layer is not suitable as a seed layer for subsequent electroplating processes, a separate seed layer is applied over the surface of the barrier layer. One or more copper elements are then electroplated on selected portions of the seed layer or, if suitable, the barrier layer. If used, the seed layer is then substantially removed. At least a portion of a surface of the barrier layer is rendered unplatable while leaving the copper elements suitable for electroplating. A protective layer is then electroplated onto surfaces of the one or more copper elements.

A tool architecture for implementing the foregoing process is also set forth. The disclosed tool architecture may be used to minimize the number of wafer movements between the tool sets required to form a complete metallization layer structure.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Fig. 1 is a process flowchart illustrating one manner of implementing a dual-damascene interconnect architecture.

Fig. 2 illustrates a tool set architecture and corresponding workpiece movements for implementing the process shown in Fig. 1.

Fig. 3 illustrates one manner of configuring tool sets for the tool set architecture of the present invention.

Fig. 4 is a process flow chart illustrating one manner of implementing an interconnect metallization structure using a minimal number of workpiece movements between the tool sets of Fig. 3.

Figs. 5A – 5K illustrate an interconnect metallization structure formed using the process of Fig. 4 at the various stages of the metallization level development.

Fig. 6 illustrates a tool set architecture and corresponding workpiece movements for implementing the process shown in Fig. 4.

Fig. 7 illustrates a tool set architecture and corresponding workpiece movements for implementing the process shown in Fig. 4 wherein an inspection tool set is used to check the semiconductor workpieces at intermediate stages of the metallization processing.

Figs. 8 illustrates one manner of configuring tool set configuration for implementing another process architecture of the present invention in which a

hard mask is used for interconnect patterning.

Figs. 9 and 10 illustrate specific embodiments of tools sets that may be used in the tool set configuration of Fig. 8.

Fig. 15 is a process flow chart illustrating one manner of forming an interconnect metallization structure using a minimal number of workpiece movements between the tool sets shown in Fig. 8.

Figs. 12 - 14 illustrate an interconnect metallization structures formed using the process of Fig. 11 at selected stages of the metallization level development.

Fig. 15 is a process flow chart illustrating a further manner of implementing an interconnect metallization structure using a minimal number of workpiece movements and hard mask patterning.

Fig. 16 illustrates a tool set configuration and corresponding workpiece movements for implementing the process shown in Fig. 15.

Figs. 17 and 18 illustrate an interconnect metallization structure formed using the process of Fig. 15 at selected stages of the metallization level development.

Figs. 19 and 20 illustrate a tool set configuration and corresponding workpiece movements for implementing the processes shown in Figs. 11 and 15, respectively, wherein an inspection tool set is used to check the workpieces at intermediate stages of the metallization processing.

DETAILED DESCRIPTION OF THE INVENTION

A basic understanding of certain terms used herein will assist the reader in understanding the disclosed subject matter. To this end, basic definitions of certain terms, as used in the present disclosure, are set forth below.

Single Metallization Level is defined as a composite level of a workpiece that is exterior to the substrate. The composite level comprises one or more interconnect lines and one or more interconnect posts that are substantially covered by a dielectric layer so that the dielectric layer insulates selected interconnect lines and interconnect posts that are not designed to be interconnected from one another.

Substrate is defined as a base layer of material over which one or more metallization levels are disposed. The substrate may be, for example, a semiconductor wafer, a ceramic block, etc.

Workpiece is defined as an object that at least comprises a substrate, and may include further layers of material or manufactured components, such as one or more metallization levels, disposed on the substrate.

The present invention employs a novel approach to applying copper metallization to a workpiece, such as a semiconductor article. The approach results in a copper metallization level that is readily manufactured using a minimal number of processing tool sets and a minimal number of workpiece

movements between the tool sets. The manufacturing process steps used to construct the resulting copper interconnect level avoids many of the inherently problematic processing steps associated with damascene interconnect structures. For example, seed layers, copper metallization layers, and barrier layers no longer need to be deposited into high aspect ratio trenches and vias using non-conformal vapor deposition processes. Rather, the barrier and metal seed layers are preferably applied to the workpiece in a blanket deposition process over planarized surfaces of the workpiece. Subsequent deposition of the copper metallization used to form at least the lines is accomplished using an electrochemical deposition process in which the copper is deposited beginning at the bottom of an opening in a patterned hard mask layer, thereby ensuring that the resulting line is completely formed and eliminating the pinch-off problems associated with the three-dimensional filling of the trench and via employed in damascene processing. Similarly, deposition of the copper metallization used to form the posts is accomplished using an electrochemical deposition process in which the copper is deposited beginning at the bottom of an opening in either a patterned hard mask layer or a patterned photoresist layer. Further, chemical mechanical polishing processes may be avoided in favor of electrochemical planarization and/or etching processes.

Manufacturing of the disclosed interconnect level architecture is accomplished with a minimal number of workpiece processing tool sets and with a minimal number of workpiece movements between the tool sets. As such, the

cost of capital equipment in the design of a manufacturing facility used for the generation of such interconnects structures may be minimized. Further, by reducing the number of workpiece movements between the tool sets, the risk of damage to the workpieces is substantially decreased.

The basic tool sets for implementing a tool architecture in accordance with one embodiment of the present invention is illustrated in Fig. 3. As shown, the tool sets comprise a film deposition tool set 20, a pattern processing tool set 25, a wet processing tool set 30, and a dielectric processing tool set 35.

In the disclosed embodiment of Fig. 3, the film deposition tool set 20 is preferably a vacuum deposition tool set. As will become apparent from the subsequent discussion of the processing operations performed on the semiconductor workpiece, the film deposition tool set 20 deposits one or more films on generally planar surfaces of the semiconductor workpiece. Such film deposition is preferable to depositing the films in the micro-recessed features employed in damascene processing. As such, low cost vacuum deposition techniques, such as physical vapor deposition (PVD), may be employed. Chemical vapor deposition (CVD) processes may also be employed.

The particular embodiment of the film deposition tool set 20 shown in Fig. 3 includes an input station 40 disposed to receive semiconductor workpieces. The input station 40 may be configured to accept the semiconductor workpieces in multi-workpiece cassettes or in multi-workpiece or single-workpiece hygienic pods. Semiconductor workpieces are transferred from the input station 40 to a

plurality of processing stations. Preferably, the semiconductor workpieces are first transferred to a conditioning station 45 where the surface of a generally planar dielectric layer disposed exterior to the semiconductor workpiece substrate is treated to enhance adhesion of a subsequent film layer. Such adhesion enhancement of the dielectric layer can be accomplished using any one or more known dry chemical processes. Depending on the characteristics of the dielectric layer and the subsequent film layer, adhesion enhancement may not be necessary. In such instances, the conditioning station 45 need not be included in the film deposition tool set 20.

Each semiconductor workpiece is then provided to a bonding film application station 50 where an optional bonding layer is applied exterior to (preferably, directly on) the dielectric layer. Materials suitable for the bonding layer include aluminum, titanium, and chromium. Preferably, such materials for the bonding layer are deposited using a vapor deposition technique, such as PVD or CVD. Depending on the properties of adjacent film layers, the bonding layer may not be desired and, as such, the bonding film application station 50 need not be included in the film deposition tool set 20.

A barrier layer application station 55 is disposed within the film deposition tool set 20 to apply a barrier layer material exterior to the dielectric material of the semiconductor workpiece. Depending on properties of other materials incorporated within the interconnect structure, the barrier layer may be comprised of tantalum, tantalum nitride, titanium nitride, titanium oxynitride,

titanium-tungsten alloy, or tungsten nitride. Particularly when the interconnect level makes contact to terminals of semiconductor devices, it is advantageous to employ a composite barrier comprised of two layers, as taught by Stevens in U.S. Patent No. 4,977,440 and in U.S. Patent No. 5,070,036. The barrier layer may be formed using a vacuum deposition process such as PVD or CVD.

To augment the conductivity of the barrier layer and to provide for good adhesion of subsequently formed layers, the film deposition tool set 20 preferably includes a seed layer application station 60. The seed layer application station 60 preferably deposits the seed layer using a PVD or CVD process. The seed layer is preferably copper, but seed layers may also be comprised of metals such as nickel, iridium, platinum, palladium, chromium, vanadium, or other conductive materials such as iridium oxide. After the seed layer has been applied, the semiconductor workpieces are transferred to an output station 62 for subsequent transfer to other semiconductor processing tool sets.

The pattern processing tool set 25 includes a plurality of processing stations which are used to provide an interconnect line pattern over the seed layer applied by the film deposition processing tool set 20. The pattern processing tool set 25 is also used to provide a post pattern over the interconnect metallization that is formed using the interconnect line pattern. As will be set forth in further detail below, the interconnect line pattern defines the regions in which primary conductor paths are provided for horizontal electrical interconnection in a plane of the semiconductor workpiece, while the post pattern defines the regions in

which primary conductor paths are provided for vertical electrical connections between adjacent planes of the semiconductor workpiece.

In the tool set embodiments illustrated in Fig. 3, the pattern processing tool set 25 is a photolithography tool set. The pattern processing tool set 25, as such, includes an input station 65 receiving semiconductor workpieces in multi-workpiece cassettes or in single-workpiece or multi-workpiece hygienic pods. The semiconductor workpieces undergo standard photolithographic conditioning, coating, and baking processes at processing stations 70, 75, and 80, respectively. After the photoresist is baked onto the semiconductor workpiece at station 80, the workpiece is transferred to the input station 85 of a photoresist exposure apparatus 90. The photoresist exposure apparatus 90 may be, for example, a step and repeat apparatus that exposes the photoresist to ultra-violet light in a manner that selectively affects the photoresist layer so that portions of the photoresist layer may be subsequently removed to form the interconnect line or post patterns.

After processing in the photoresist exposure apparatus 90, the semiconductor workpiece is provided to the output station 95 of the apparatus 90 for transfer to further processing stations that selectively remove the photoresist layer to form a pattern in the layer consistent with the pattern exposure in the photoresist exposure apparatus 90. Such processing stations include a photoresist development station 100 and a plasma cleaning ("de-scum") station 105. After selective removal of the photoresist layer and plasma cleaning, the semiconductor workpieces may be transferred to an output station 110 or, optionally, to an

intermediate UV cure station 107 and therefrom to output station 110 for provision to one or more further tool sets.

The wet processing tool set 30 implements a wide range of processes used to form the interconnect line metallization and post metallization structures. The wet processing tool set 30 may be implemented in an LT-210™ brand copper plating tool available from Semitool, Inc., of Kalispell, Montana. Such a wet processing tool set preferably includes input station 115 for receiving semiconductor workpieces in multi-workpiece cassettes or in single-workpiece or multiple-workpiece pods, and an output station 120 for supplying processed workpieces in pods or cassettes to one or more subsequent tool sets. Stations 115 and 120 are preferably combined into a single input/output station. Dual robot arms 125a and 125b are disposed for travel in the direction of arrows 130 and are used to transfer the semiconductor workpieces between a plurality of processing stations and to and from the output station 120 and input station 115.

The processing stations of the wet processing tool set 30 perform at least three primary wet processing operations. First, the wet processing tool set 30 includes processing stations used to apply copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed by the pattern processing tool set 25. To this end, electrochemical deposition stations 135 and 140 are provided. Additionally, a conditioning station 145 may be employed to condition surfaces of the semiconductor workpiece that are to be electrochemically deposited with copper. Second, the wet processing

tool set 30 includes one or more processing stations used to remove the material that is used to form the interconnect line pattern and the post pattern that is applied by the pattern processing tool set 25. Processing station 150 and rinse/dry stations 155 and 160 are included for this purpose. Finally, one or more processing stations are employed to either remove portions of the seed layer and/or barrier layer that are not overlied by interconnect lines of metallization and/or to otherwise render such portions non-conductive. As will be set forth in further detail below, oxidizing station 165, etching station 170, and electrochemical removal station 175 may be used for such seed layer and barrier layer processing. Oxidizing station 165 and etching station 170 may be consolidated into a single processing station.

Optionally, the processing tool 30 may be used to apply a protective coating over the interconnect line metallization and post metallization. In the illustrated embodiment, electrochemical deposition station 180 may be used for this purpose. Materials for the protective coating are preferably those which impede both copper migration into the dielectric and oxidation of the coated copper. Materials that may be employed for the protective coating include, for example, nickel, nickel alloys and chromium.

The dielectric processing tool set 35 includes a plurality of processing stations that are used to deposit a dielectric layer over the interconnect line metallization and post metallization. Additionally, the dielectric processing tool set 35 includes one or more processing stations for etching the deposited

dielectric layer to expose upper connection regions of the post metallization. In the illustrated embodiment, the dielectric processing tool set 35 includes an input station 185 that is adapted to receive semiconductor workpieces in multi-workpiece cassettes or in single-workpiece or multiple-workpiece hygienic pods. Semiconductor workpieces are provided from the input station 185 to a coating station 190 where the surface of each semiconductor workpiece is coated with a dielectric precursor or the like. After a workpiece has been coated, it is sequentially supplied to a baking station 195 and a curing station 200 to complete formation of a dielectric material that surrounds the interconnect line metallization and post metallization. The semiconductor workpiece is then supplied to an etch back station 205 where the upper surface of the dielectric layer is etched back to expose upper connection regions of the post metallization.

Referring again to Fig. 3, the separate input and output stations 40 and 62 for tool set 20 may optionally be combined in a single input/output station. Similarly, separate input and output stations 65 and 110 of tool set 25 may optionally be combined in a single input/output station, and the single input/output station 115 for tool set 30 may optionally be divided into separate input and output stations. One or more cassettes or pods may be resident in the the input/output stations at any time. Separate input and output stations 185 and 210 for tool set 35 may also optionally be combined in a single input/output station.

With reference to Fig. 6, the processing tool sets described in connection

with Fig. 3 may be used to implement the manufacturing process procedures described below in connection with Fig. 4 with a minimal number of workpiece movements between the tool sets. Process steps 215, 225, 237 and 260 of Fig. 4 may be implemented in the film deposition tool set 20. Process steps 270 and 300 may be implemented in the pattern processing tool set 25. Process steps 280, 290, and 308 through 380 may be implemented in the wet processing tool set 30. Process steps 400 through 425 are implemented in the dielectric processing tool set 35.

As a result of the particular processing steps utilized and the allocation of the processing steps among the various tool sets, a single interconnect metallization level may be formed with no more than ten and, preferably no more than five workpiece movements between the tool sets, substantially less than the 13 workpiece movements required for the dual-damascene process described above. To this end, a single workpiece movement, designated at arrow 500 of Fig. 6, is employed for transferring the workpieces between the film deposition tool set 20 and the pattern processing tool set 25. Three workpiece movements, designated at arrows 505, 510, and 515, are employed to transfer the workpieces between the pattern processing tool set 25 and the wet processing tool set 30. A single workpiece movement, designated at arrow 520, is employed to transfer the workpieces between the wet processing tool set 30 and the dielectric processing tool set 35. As such, there is a substantial reduction in the number of workpiece movements between the tool sets when compared to the traditional dual-

damascene processing and tool architecture of Figs. 1 and 2.

One embodiment of the basic process employed to form the disclosed metallization structure so as to minimize workpiece movements between the tool sets is set forth in the flow chart of Fig. 4 while the corresponding formation of one embodiment of the metallization structure at various processing states is illustrated in Fig. 5A – 5K. As shown in Figs. 4 and 5A, a dielectric layer 210 is provided over a substrate 215, such as a semiconductor wafer. Although not specifically shown in Fig. 5A, the dielectric layer 210 likely includes contacts to metal-filled vias exposed at the top of the dielectric layer that have been planarized and that provide an electrical connection between one or more components below the planarized surface of the dielectric layer. The one or more components below the planarized surface of the dielectric layer may include a further interconnect metallization level, a direct connection to a semiconductor component formed in the substrate, etc. The dielectric layer 210 preferably has a relative permittivity of less than 4 and may be formed by spin application or spray application of a precursor material or precursor materials followed by a cure, in either an anaerobic or in an oxygen-containing atmosphere, at a temperature of less than 450C. A preferred choice for the dielectric material is benzocyclobutene (BCB).

Preferably, the surface of the dielectric layer 210 is conditioned, as at step 215, to enhance the adhesion of a subsequently applied layer. The surface of the dielectric layer 210 may be conditioned using wet or dry chemical processes or

through an ion milling process. The arrows 220 in Fig. 5A depict conditioning of the upper surface of the dielectric layer 210 by, for example, impinging argon or nitrogen ions. Alternatively, the upper surface may be conditioned by a brief (10 to 30 second) etch in a solution comprised of 1% to 2% hydrofluoric acid in deionized water.

As illustrated at Fig. 5B and at step 225 of Fig. 4, an optional bonding layer 230 may be applied to the surface of the dielectric layer 210. The bonding layer 230 may be comprised of, as noted above, aluminum, titanium, or chromium which has been deposited using a vapor deposition technique such as PVD.

At step 237 of Fig. 4, a barrier layer 240 is deposited over the bonding layer 230, if used, or directly onto the surface of the dielectric layer 210. The barrier layer 240, as illustrated, is deposited over a generally planar surface of a semiconductor workpiece thereby eliminating the need to apply the barrier layer material into high aspect ratio trenches and vias. Depending on the properties of other materials incorporated within the interconnect structure, the barrier layer 240 may be comprised of tantalum, tantalum nitride, titanium nitride, titanium oxynitride, titanium-tungsten alloy, or tungsten nitride. As noted above, a composite barrier comprised of two layers, as taught by Stevens in U.S. Patent No. 4,977,440 and in U.S. Patent No. 5,070,036 may be used for contact to semiconductor device contacts. It is noted that a deposited bonding layer is not required to achieve acceptable adhesion between a tantalum barrier layer and a

properly-conditioned BCB surface of the dielectric layer 210.

The barrier layer 240 may be made to be sufficiently conductive to facilitate a subsequent electrochemical deposition process for depositing interconnect line and post metallization. However, if the conductivity of the barrier layer 240 is insufficient, a seed layer may be required.

Fig. 5B and step 260 of Fig. 4 illustrate application of a seed layer 265 that is deposited, for example, in a PVD or CVD process. The seed layer 265 is typically copper, but may also be comprised of metals such as nickel, iridium, platinum, palladium, chromium, vanadium or other conductive materials such as iridium oxide. Preferred thicknesses for the seed and barrier layers are in the range of 200 to 600 Å.

Referring again to Fig. 5B and step 270 of Fig. 4, procedures well-established in the photolithographic arts may be employed to deposit the interconnect line pattern using, for example, photoresist 272 as a mask. In such instances, a plasma treatment may be included as a final step in the photolithographic procedure or at any processing stage prior to the electrochemical deposition of the interconnect line metallization in order to remove photoresist residues from exposed portions of the seed layer surface. A treatment in HMDS may be employed to form a layer 270 that promotes adhesion between photoresist and the copper seed layer 265. Additionally, or alternatively, a thin (less than 100 Å) layer of copper oxide may be formed on the upper surface of the seed layer 265 to form layer 270 and thereby promote adhesion

between the seed layer and photoresist.

Referring to Fig. 5C and step 280 of Fig. 4, interconnect line metallization 285 is formed by selective electrochemical deposition of, for example, copper into the photoresist interconnect pattern. An acidic chemical bath is preferably employed for the electrochemical depositions. The chemical bath may be prepared by adding copper sulfate and sulfuric acid to deionized water. As is well known in the metals-plating arts, small concentrations of materials which affect metal grain size and film conformability may optionally be included in the chemical bath.

After the interconnect metallization 285 has been deposited into the photoresist interconnect pattern, the photoresist is removed. Removal of the photoresist may be accomplished by exposing the photoresist to a solvent or oxidant (such as ozonated DI water) followed by a rinse in water. Such a step is illustrated at steps 290 and 295 of Fig. 4 and should be sufficient to remove photoresist after selective metal depositions. The resultant structure is shown in Fig. 5D.

As illustrated at Fig. 5E and at step 300 of Fig. 4, a further photoresist pattern 305 is applied to the semiconductor workpiece in order to form openings through which the post metallization 307 may be electrochemically deposited as at step 308. A metallized post 307 is shown in Fig. 5F. After the post metallization has been deposited, the photoresist pattern is removed thereby leaving the interconnect structure of Fig. 5G.

Referring now to Fig. 5H and to steps 315, 320, and 325 of Fig. 4, the seed layer 265 is partially or completely removed by, for example, an electrochemical etching process. Electrochemical etching may be accomplished by exposing the seed layer to a suitable electrolyte solution, such as a solution containing phosphoric acid, while the seed layer 265 is held at a positive electrical potential relative to an electrode that is immersed in the electrolyte solution.

Shown in Fig. 5H is a representative cross section after partial removal of the exposed seed layer followed by formation of copper tantalum oxide on the exposed surface of the barrier layer and formation of copper oxide on exposed surfaces of lines and posts. As detailed above, the seed layer 265 may be partially removed by immersion in electrolyte solution which contains phosphoric acid while the seed layer is held at a positive electrical potential relative to an electrode that is immersed in the same electrolyte solution. The seed layer that remains after electrochemical etching is then converted to copper oxide. Alternatively, when the seed layer thickness is less than about 10% of minimum line width, the electrochemical etch may be omitted and the seed layer may be completely converted to copper oxide.

Referring to step 320, exposed surfaces of the copper structures 285, 307, and 265 and the barrier layer 240 are oxidized by exposure to a solution comprised of air, oxygen, steam, water including dissolved oxygen, or ozone dissolved in water. Alternatively, the surfaces may be oxidized by heating in an

oxygen containing atmosphere. As illustrated at step 325, the resultant copper oxide may be removed by exposure to a solution which contains sulfuric acid, hydrochloric acid, or both sulfuric and hydrochloric acid. Referring to Fig. 3, copper oxide removal may be accomplished at station 145 of tool set 25.

A protective coating 370 is preferably provided over the remaining interconnect structures. Such a protective coating is preferably formed in an electrochemical process, such as at steps 375, that causes a material to deposit on the exposed copper but not on the oxide-coated, exposed barrier material. Materials for the protective coating preferably include those which impede copper migration into the dielectric and, further, which impede oxidation of the coated copper. Such materials include nickel, nickel alloys and chromium. Preferred thicknesses for the protective coating are in the range of 50Å to 500Å. The resultant structure is shown at Fig. 5I.

Referring to step 380 of Fig. 4, the barrier layer 240 and its overlying oxide layer may be removed where it is not covered by an overlying copper feature by a wet-chemical etch. The wet chemical etch may comprise a solution of 1% to 5% hydrofluoric acid in water, provided that the barrier removal procedure does not excessively attack either copper features of the interconnect structure 302 or the dielectric 210 that underlies the barrier layer 240.

As illustrated at Fig. 5J and at steps 400 and 405 of Fig. 4, a further dielectric layer 410 is formed to a thickness sufficient to cover the upper surfaces of the posts of the interconnect structure. The further dielectric layer 410 is

preferably formed by spin application or spray application of a precursor material or precursor materials followed by a cure, in either an anaerobic or in an oxygen-containing atmosphere, at a temperature of less than 450C. Composition of the dielectric layer 410 may be different than or the same as the composition of the dielectric layer 210.

After the further dielectric layer 410 has been cured, the upper surface of the layer 410 is etched back to expose upper contact regions 420 of the post structure 307. For example, a blanket plasma etch may be employed to reduce the thickness of layer 410 until all upper surfaces 420 of the post structures 307 are exposed. Etching of BCB, for example, may be done in a plasma that contains oxygen and fluorine ions. Such a step is illustrated at step 425 of Fig. 4 and the resulting structure is shown at Fig. 5K.

A further embodiment of a tool architecture suitable for implementing the foregoing process steps is illustrated in Fig. 7. The tool architecture illustrated in Fig. 7 is similar to the specific embodiment of the tool sets shown in Fig. 3 as incorporated in the tool architecture of Fig. 6 (although it will be recognized that the more generic processing tools set designations of Fig. 6 may likewise be used in Fig. 7 without incorporating the specific tool set implementations disclosed in Fig. 3). However, the tool architecture of Fig. 7 includes an inspection tool set 600 that is used to check the semiconductor workpieces at intermediate stages of the application of a single metallization level. The intermediate checks are used, for example, to insure proper registration of the various photoresist patterns and

corresponding metallization and, further, to insure proper dielectric etch-back. As such, each semiconductor workpiece may be provided to the inspection tool set 600 after processing steps 270, 290, 300, 380 and 425 that are illustrated in Fig. 4. In the illustrated embodiment, ten workpiece movements are used to transfer the semiconductor workpiece between the various tools of the tool processing architecture to form a single interconnect metallization level. The inspection tool set 600 may be implemented, for example, with inspection devices available from KLA-Tencor.

TOOL ARCHITECTURE AND PROCESS USING HARD MASK PATTERNING

At least four embodiments of a process for manufacturing a metallization level using hard mask patterning are disclosed. In a first embodiment, only the interconnect metallization pattern is formed using a hard mask dielectric layer. In a second embodiment, both the interconnect metallization pattern and the post pattern are formed using hard mask dielectric layers. The third and fourth process embodiments are respectively similar to the first and second process embodiments, except that intermediate inspections are performed during the processing to ensure proper formation of the interconnect line and post patterns. Processing architectures, processing tool sets, and workpiece movements are set forth with respect to each of the process embodiments.

The basic tool sets for implementing a process architecture in accordance

with one embodiment of the present invention are illustrated in Fig. 8. As shown, the tool sets comprise a film deposition tool set 1020, a hard mask formation tool set 1023, a pattern processing tool set 1025, a hard mask etch tool set 1027, an electrochemical/wet processing tool set 1030, and a dielectric processing tool set 1035.

In the disclosed embodiment of Fig. 8, the film deposition tool set 1020 is preferably a vacuum deposition tool set. As will become apparent from the subsequent discussion of the processing operations performed on the workpiece, the film deposition tool set 1020 deposits one or more films on generally planar surfaces of the workpiece. Such film deposition is preferable to depositing the films in the micro-recessed features employed in damascene processing. As such, low cost vacuum deposition techniques, such as physical vapor deposition (PVD), may be employed. Chemical vapor deposition (CVD) processes may also be employed.

A particular embodiment of the film deposition tool set 1020 shown in Fig. 9 includes a plurality of processing stations for conditioning a surface of the workpiece, depositing a bonding layer, depositing a barrier layer, and depositing a seed layer on the workpiece. Preferably, the workpieces are first transferred to a conditioning station where the surface of a generally planar dielectric layer disposed exterior to the workpiece substrate is treated to enhance adhesion of a subsequent film layer. Such adhesion enhancement of the dielectric layer can be accomplished using any one or more known plasma processes. Depending on the

characteristics of the dielectric layer and the subsequent film layer, adhesion enhancement may not be necessary. In such instances, a conditioning station need not be included in the film deposition tool set 20. Each workpiece is then provided to a bonding film application station where an optional bonding layer is applied exterior to (preferably, directly on) the dielectric layer. Materials suitable for the bonding layer include aluminum, titanium, and chromium. Depending on the properties of adjacent film layers, the bonding layer may not be desired and, as such, a bonding film application station need not be included in the film deposition tool set 1020. A barrier layer application station is used to apply a barrier layer material exterior to the dielectric material of the workpiece. Depending on properties of other materials incorporated within the interconnect structure, the barrier layer may be comprised of tantalum, tantalum nitride, titanium nitride, titanium oxynitride, titanium-tungsten alloy, or tungsten nitride. Particularly when the interconnect level makes contact to terminals of semiconductor devices, it is advantageous to employ a composite barrier comprised of two layers, as taught by Stevens in U.S. Patent No. 4,977,440 and in U.S. Patent No. 5,070,036.

To augment the conductivity of the barrier layer and to provide for good adhesion of subsequently formed layers, the film deposition tool set 1020 preferably includes a seed layer application station. The seed layer application station preferably deposits the seed layer using a PVD or CVD process. The seed layer is preferably copper. After the seed layer has been applied, the workpieces

are transferred to an output station for subsequent transfer to other processing tool sets.

The hard mask formation tool set 1023 includes a plurality of processing stations which are used to provide a hard mask dielectric layer over the seed layer applied by the film deposition processing tool set 1020. This hard mask dielectric layer is ultimately patterned in accordance with a photoresist pattern applied by the pattern processing tool set 1025. One or more hard mask layers are applied to provide the patterned masks used for depositing one or both of the interconnect line and post metallization. As will be set forth in further detail below, the interconnect line pattern defines the regions in which primary conductor paths are provided for horizontal electrical interconnection in a plane of the workpiece, while the post pattern defines the regions in which primary conductor paths are provided for vertical electrical connections between adjacent planes of the workpiece.

In the particular tool set embodiment illustrated in Fig. 10, the hard mask formation tool set 1023 includes an input station 1465 that preferably receives the workpieces in multi-workpiece cassettes or in single-workpiece or multi-workpiece hygienic pods. From the input station 1465, a workpiece is provided to a coating station 1467 where the workpiece is coated with one or more precursor materials. The workpiece is then provided to a baking station 1470 to, for example, bake out solvents. The baking station 1470 is typically a hot plate. After processing at the baking station 1470, the workpiece is provided to a cure

station 1473. Depending on the duration of the cure cycle, the cure station 1473 may be a hot plate or a small batch furnace. The curing cycle must not cause damage to the workpiece. After curing, the workpiece is provided to the output station 1475. Although the illustrated embodiment is shown with separate input and output stations, the stations may be combined into a single input/output station.

The pattern processing tool set 1025 of Fig. 8 includes a plurality of processing stations which are used to provide an interconnect line pattern over the hard mask layer applied by the hard mask formation tool set 1023. In accordance with one of the disclosed processes, the pattern processing tool set 1025 is also used to provide a post pattern over the interconnect metallization that is formed using the interconnect line pattern. Alternatively, as will be set forth below, the pattern processing tool set 1025 is used to provide a post pattern over a further hard mask layer deposited by the hard mask formation tool set 1023 which, in turn, provides a mask for the deposition of the post metallization.

In the tool set embodiment illustrated in Fig. 9, the pattern processing tool set 1025 is a photolithography tool set. The pattern processing tool set 1025, as such, includes an input station receiving workpieces, such as semiconductor wafers, in multi-workpiece cassettes or in single-workpiece or multi-workpiece hygienic pods. Within tool set 1025 the workpieces sequentially undergo the standard photolithographic processes of conditioning, coating, and baking. After the photoresist is baked onto the workpiece, the workpiece is transferred to the

input station of a photoresist exposure apparatus such as a step and repeat apparatus that exposes the photoresist to ultra-violet light in a manner that selectively affects the photoresist layer so that portions of the photoresist layer may be subsequently removed to form the interconnect line or post patterns. After exposure of the photoresist layer, the workpiece is provided to an output station for transfer to further processing stations that selectively remove the photoresist layer to form a pattern in the layer consistent with the pattern exposure in the photoresist exposure apparatus. Such processing stations include a photoresist development station and may include a plasma cleaning ("de-scum") station. After selective removal of the photoresist layer and plasma cleaning, the workpieces are transferred to an output station for provision to one or more further tool sets.

As shown in Fig. 9, the hard mask etch tool set 1027 includes an input station 1480 that preferably receives the workpieces in multi-workpiece cassettes or in single-workpiece or multi-workpiece hygienic pods. From the input station 1480, a workpiece is provided to an etching station 1483 where the hard mask layer is selectively etched through open regions of the patterned photoresist layer applied by the pattern processing tool set 1025. After the hard mask layer has been etched to form the desired mask pattern, the workpiece is provided to output station 1485. Although the embodiment shown in Fig. 10 illustrates separate input and output stations, a single input/output station may be used. The hard mask etch tool set 1027 may be a plasma etch apparatus such as one sold by

Tegal, Applied Materials, or LAM Research.

The electrochemical/wet processing tool set 1030 of Fig. 8 implements a wide range of processes used to form the interconnect line metallization and post metallization structures. The wet processing tool set 1030 may be implemented in an Equinox™ brand tool or an LT-210™ brand tool, both of which are available from Semitool, Inc., of Kalispell, Montana. As illustrated in Fig. 9, such an electrochemical/wet processing tool set preferably includes input and output stations and a plurality of stations for performing electrochemical and wet chemical processes. The processing stations of the wet processing tool set 30 perform at least three primary wet processing operations. First, the wet processing tool set 30 includes processing stations used to apply copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed using the pattern processing tool set 25 and/or the hard mask etch tool set 1027. Additionally, a conditioning station may be employed to condition surfaces of the workpiece that are to be electrochemically deposited with copper. Second, the tool set 30 includes one or more processing stations used to remove the hard mask material that is used to define the interconnect line pattern and, in some process embodiments, the post pattern that is applied by the hard mask formation tool set 1023 and etched by the hard mask etch tool set 1027. Similarly, the wet processing tool set 30 includes one or more processing stations used to remove the photoresist material that is employed to define the interconnect line pattern in the hard mask layer and, in

some process embodiments, the photoresist material that is employed to define the post pattern. Typically, a solvent station and rinse/dry stations are provided for photoresist removal. Finally, one or more processing stations are employed to either remove portions of the seed layer and/or barrier layer that are not overlied by interconnect lines and/or to otherwise render such portions non-conductive.

Optionally, the processing tool 30 may be used to apply a protective coating over the interconnect line metallization and post metallization. In one specific embodiment, an electrochemical deposition station may be used for this purpose. Materials for the protective coating are preferably those which impede both copper migration into the dielectric and oxidation of the coated copper. Materials that may be employed for the protective coating include, for example, nickel, nickel alloys and chromium.

The dielectric processing tool set 1035 includes a plurality of processing stations that are used to form a dielectric layer over the interconnect line metallization and post metallization. Additionally, the dielectric processing tool set 1035 includes one or more processing stations for etching the deposited dielectric layer to expose upper connection regions of the post metallization. With respect to the specific embodiment of the dielectric processing tool set shown in Fig. 9, the workpieces are provided from an input station to a coating station where the surface of each workpiece is coated with a dielectric precursor or the like. After a workpiece has been coated, it is sequentially supplied to a baking station and a curing station to complete formation of a dielectric material

that surrounds the interconnect line metallization and post metallization. The workpiece is then supplied to an etch back station where the upper surface of the dielectric layer is etched back to expose upper connection regions of the post metallization.

With reference to Fig. 8, the processing tool sets may be used to implement the manufacturing process procedures described below in connection with Fig. 11 with a minimal number of workpiece movements between the tool sets. Process steps 1215, 1225, 1237 and 1260 of Fig. 11 may be implemented in the film deposition tool set 1020. Process steps 1270 and 1308 may be implemented in the pattern processing tool set 1025. Process steps 1277, 1280, and 1309 through 1380 may be implemented in the wet processing tool set 1030. Process steps 1400 through 1425 are implemented in the dielectric processing tool set 1035. Process step 1261 may be implemented in the hard mask formation tool set 1023, and process step 1273 may be implemented in the hard mask etching tool set 1027.

As a result of the particular processing steps utilized and the allocation of the processing steps among the various tool sets, a single interconnect metallization level may be formed with no more than seven workpiece movements between the tool sets when a hard mask is used to pattern only the interconnect lines. When a hard mask is used to pattern both the interconnect lines and the posts, a single interconnect metallization level, as shown in Fig. 16, may be formed with no more than nine workpiece movements.

To this end, a single workpiece movement, designated at arrow 1500 of Fig. 8, is employed for transferring the workpieces between the film deposition tool set 1020 and the hard mask formation tool set 1023. One workpiece movement, designated at arrow 1505, is employed to transfer the workpieces between the hard mask formation tool set 1023 and the pattern processing tool set 1025. Two workpiece movements 1510 and 1512 are used to transfer the workpieces between the pattern processing tool set 1025 and the wet processing tool set 1030. A single workpiece movement 1515 is used to transfer the workpieces between the pattern processing tool set 1025 and the hard mask etching tool set 1027. Similarly, a single workpiece movement 1517 is used to transfer the workpieces between the hard mask etching tool set 1027 and the wet processing tool set 1030. Finally, a single workpiece movement 1520 is employed to transfer the workpieces between the wet chemical processing tool set 1030 and the dielectric processing tool set 1035. As such, there is a substantial reduction in the number of workpiece movements between the tool sets when compared to the traditional dual-damascene processing architecture and tool configuration of Figs. 1 and 2.

At step 1261 of Fig. 11, a hard mask dielectric layer 1263 is deposited over the seed layer 1265 at the hard mask formation tool set 1023. In step 1270 of Fig. 11, procedures well-established in the photolithographic arts may be employed to deposit the interconnect line pattern over the hard mask dielectric layer 1263 using, for example, photoresist as an intermediate mask. The hard

mask dielectric layer 1263 is then selectively etched through open portions of the photoresist layer 1272 as shown by step 1273. Step 1273 takes place at the hard mask etching station 1027. With reference to step 1277 of Fig. 11, the photoresist layer 1272 is removed at a wet chemical processing station within tool set 1030 thereby leaving a patterned hard mask dielectric layer 1263 having substantially vertical walls for defining the interconnect metallization pattern.

Referring to step 1280 of Fig.11, interconnect line metallization 1285 is formed by selective electrochemical deposition of, for example, copper into the hard-mask interconnect pattern. An acidic chemical bath is preferably employed for the electrochemical depositions. The chemical bath may be prepared by adding copper sulfate and sulfuric acid to deionized water. As is well known in the metals-plating arts, small concentrations of materials which affect metal grain size and film conformability may optionally be included in the chemical bath.

The structure that results after the electrochemical deposition of the copper is illustrated in Fig. 12. In Fig. 12, the generally planar surface of the workpiece is illustrated at 1210, a conditioned portion of the workpiece is illustrated at 1230, the barrier layer is illustrated at 1240, the hard mask layer is illustrated at 1263, the seed layer is illustrated at 1265, and an exemplary interconnect metallized line is illustrated in cross-section at 1285.

After the interconnect metallization has been deposited into the patterned hard mask dielectric layer, the workpiece may be returned to the pattern processing tool set 1025 where the pattern for the post metallization is formed

using, for example, a photoresist layer that is applied and patterned using conventional photoresist patterning techniques. As at step 1308, this further photoresist pattern is applied to the workpiece in order to form openings through which the post metallization may be electrochemically deposited. Fig. 13 illustrates the structure that results after patterning of a photoresist layer 1305 and electrochemical deposition of the post metallization 1307 at step 1309 of Fig. 11.

After the post metallization has been deposited at step 1309, the photoresist pattern is removed at step 1310 and the hard mask dielectric layer is removed at step 1313. Removal of the hard mask dielectric layer preferably takes place within tool set 1030, but may also take place at the hard mask etching tool set 1027 with the addition of two further wafer movements.

The hard mask dielectric layer 1263 may be removed prior to the formation of the patterned photoresist layer. Fig. 14 illustrates the structure that results after patterning of a photoresist layer 1305 and electrochemical deposition of the post metallization 1307. In such instances, a treatment in HMDS may be employed to form a layer that promotes adhesion between photoresist 305 and the copper seed layer 1265. Additionally, or alternatively, a thin (less than 100 Å) layer of copper oxide may be formed on the upper surface of the seed layer 1265 to form layer 1278 and thereby promote adhesion between the seed layer and photoresist.

Referring now to steps 1315, 1320, and 1325 of Fig. 11, the seed layer 1265 is partially or completely removed by, for example, an electrochemical

etching process. Electrochemical etching may be accomplished by exposing the seed layer to a suitable electrolyte solution, such as a solution containing phosphoric acid, while the seed layer 1265 is held at a positive electrical potential relative to an electrode that is immersed in the electrolyte solution.

At step 1320, exposed surfaces of the copper structures 1285, 1307, and 1265 and the barrier layer 1240 are oxidized by exposure to water including dissolved air, oxygen, or ozone. Alternatively, the surfaces may be oxidized by heating in an oxygen containing atmosphere. As illustrated at step 1325, the resultant copper oxide may be removed by exposure to a solution which contains sulfuric acid, hydrochloric acid, or both sulfuric and hydrochloric acid. Copper oxide removal may be accomplished, for example, at an etch station of tool set 30.

A protective coating is preferably provided over the remaining interconnect structures. Such a protective coating is preferably formed in an electrochemical process, such as at step 1375, that causes a material to deposit on the exposed copper but not on the oxide-coated, exposed barrier material. Materials for the protective coating preferably include those which impede copper migration into the dielectric and, further, which impede oxidation of the coated copper. Such materials include nickel, nickel alloys and chromium. Preferred thicknesses for the protective coating are in the range of 50Å to 500Å.

Referring to step 1380 of Fig. 11, the barrier layer 1240 and its overlying oxide layer may be removed where it is not covered by an overlying copper

feature by a wet-chemical etch. The wet chemical etch may comprise a dilute acid, such as solution of 1% to 5% hydrofluoric acid in water, provided that the barrier removal procedure does not excessively attack either copper line and post features 1285 and 1307 or the dielectric 1210 that underlies the barrier layer 1240.

At step 1400 of Fig. 11, a further dielectric layer is formed to a thickness sufficient to cover the upper surfaces of the posts of the interconnect structure. The further dielectric layer is preferably formed by spin application or spray application of a precursor material or precursor materials followed by a cure, in either an anaerobic or in an oxygen-containing atmosphere, at a temperature of less than 450C. Composition of the dielectric layer may be different than or the same as the composition of the dielectric layer 1210.

After the further dielectric layer has been cured, the upper surface of the layer is etched back to expose upper contact regions of the post structure 1307. For example, a blanket plasma etch may be employed to reduce the thickness of layer until all upper surfaces of the post structures 1307 are exposed. Etching of BCB, for example, may be done in a plasma that contains oxygen and fluorine ions.

In some instances, it may be desirable to use a hard mask for patterning the posts as well as the interconnect lines. One embodiment of a process that utilizes a hard mask for patterning the post structures is illustrated in Fig. 15. The corresponding wafer movements between the tool sets are illustrated in Fig. 16.

In this embodiment, the processing of the workpiece is substantially similar to the processing illustrated in Fig. 11. In terms of processing, the principal difference occurs after electrochemical deposition step 1280. In this latter embodiment, the workpiece is removed from the wet processing tool set 1030 and returned to the hard mask formation tool set 1023 wherein a further hard mask dielectric layer 1422 (Fig. 17) is disposed over the surface of the workpiece as illustrated at step 1427 of Fig. 15. After formation of the further hard mask dielectric layer 1422, the workpiece is transferred to the pattern forming tool set 1025 where, for example, a further photoresist layer 1432 is disposed over the further hard mask dielectric layer 1422 and patterned, as step 1429, in accordance with the desired post metallization pattern. The hard mask dielectric layer 1422 is then etched in accordance with this pattern at step 1443 to form the openings in which the post structures will be formed. The workpiece is then returned to the wet chemical processing tool set 1030 where the photoresist layer 1432 is stripped at step 1310 and the copper post structures are electrochemically deposited through the hard mask dielectric layer 1422 at step 1309. With reference to Fig. 18, after electrochemical deposition of the post metallization, the hard mask layers are removed, and processing proceeds in the same manner as set forth in connection with the process of Fig. 11. As illustrated in Fig. 16, the entire metallization level can be formed with nine wafer movements between the illustrated tool sets.

Further enhancements to each of the foregoing processes and tool

sets/wafer movements are illustrated in Figs. 19 and 20. The tool configurations of Figs. 19 and 20 each include an inspection tool set 600 that is used to check the workpieces at intermediate stages of the application of a single metallization level. The intermediate checks are used, for example, to insure proper registration of the various photoresist and/or hard mask patterns and corresponding metallization and, further, to insure proper dielectric etch-back. As shown in Fig. 19, each workpiece may be provided to the inspection tool set 1600 after processing steps 1270, 1280, 1308, 1380 and 1425 that are illustrated in Fig. 11. Similarly, as shown in Fig. 20, each workpiece may be provided to the inspection tool set 1600 after processing steps 1270, 1280, 1429, 1380 and 1425 that are illustrated in Fig. 16. In the embodiment illustrated in Fig. 19, twelve workpiece movements are used to transfer the workpiece between the various tools of the tool processing architecture to form a single interconnect metallization level. In the embodiment illustrated in Fig. 15, fourteen workpiece movements are used to transfer the workpiece between the various tools of the tool processing architecture to form a single interconnect metallization level. The inspection tool set 600 may be implemented, for example, with inspection devices available from KLA-Tencor.

Numerous modifications may be made to the foregoing system without departing from the basic teachings thereof. Although the present invention has been described in substantial detail with reference to one or more specific embodiments, those of skill in the art will recognize that changes may be made

thereto without departing from the scope and spirit of the invention as set forth in the appended claims.

CLAIMS

1. A manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

a film deposition tool set for depositing a barrier layer exterior to the planar dielectric surface and for depositing a seed layer exterior to the barrier layer;

a pattern processing tool set for providing an interconnect line pattern over the seed layer and for providing a post pattern over interconnect line metallization formed using the interconnect line pattern;

a wet processing tool set for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed by the pattern processing tool set,

removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern,

removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization; and

a dielectric processing tool set for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the

deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using no more than ten workpiece movements between the tool sets.

2. A manufacturing tool configuration as claimed in claim 1 wherein the wet processing tool set comprises at least one processing station for applying an electrochemically deposited protective coating exterior to the copper metallization.

3. A manufacturing tool configuration as claimed in claim 1 wherein the wet processing tool set comprises at least one processing station for conditioning a surface of the workpiece prior to further processing within the wet processing tool set.

4. A manufacturing tool configuration as claimed in claim 1 wherein the wet processing tool set comprises at least one processing station for oxidizing exposed metallized portions of the workpiece.

5. A manufacturing tool configuration as claimed in claim 4 wherein the wet processing tool set comprises at least one processing station for removing oxidized metal portions of the workpiece.

6. A manufacturing tool configuration as claimed in claim 5 wherein the at least one processing station for removing oxidized metal portions is also employed for conditioning of surfaces prior to subsequent processing.

7. A manufacturing tool configuration as claimed in claim 1 wherein the film deposition tool set is a vacuum deposition tool set.

8. A manufacturing tool configuration as claimed in claim 1 wherein the film deposition tool set deposits a substantially planar bonding layer, the barrier layer being deposited by the film deposition tool set over the bonding layer.

9. A manufacturing tool configuration as claimed in claim 1 wherein the film deposition tool set deposits a substantially planar bonding layer directly on the dielectric layer.

10. A manufacturing tool configuration as claimed in claim 1 wherein the pattern processing tool set is a photoresist processing tool set.

11. A manufacturing tool configuration as claimed in claim 1 wherein the dielectric deposition tool set deposits a low-K dielectric material.

12. A manufacturing tool configuration as claimed in claim 1 wherein the film deposition tool set is a single integrated tool.

13. A manufacturing tool configuration as claimed in claim 1 wherein the pattern processing tool set is a single integrated tool.

14. A manufacturing tool configuration as claimed in claim 1 wherein the dielectric deposition tool set is a single integrated tool.

15. A manufacturing tool configuration as claimed in claim 1 and further comprising an inspection tool set for inspecting the workpiece at one or more processing states during formation of a single metallization level.

16. A manufacturing tool configuration as claimed in claim 15 wherein the wet processing tool set comprises at least one processing station for applying an electrochemically deposited protective coating exterior to the copper metallization.

17. A manufacturing tool configuration as claimed in claim 15 wherein the wet processing tool set comprises at least one processing station for conditioning a surface of the workpiece prior to further processing within the wet processing tool set.

18. A manufacturing tool configuration as claimed in claim 15 wherein the wet processing tool set comprises at least one processing station for oxidizing exposed metallized portions of the workpiece.

19. A manufacturing tool configuration as claimed in claim 18 wherein the wet processing tool set comprises at least one processing station for removing oxidized metal portions of the workpiece.

20. A manufacturing tool configuration as claimed in claim 19 wherein the at least one processing station for oxidizing and the at least one processing station for removing oxidized metal portions are the same processing station.

21. A manufacturing tool configuration as claimed in claim 15 wherein the film deposition tool set is a vacuum deposition tool set.

22. A manufacturing tool configuration as claimed in claim 15 wherein the film deposition tool set deposits a substantially planar bonding layer, the barrier layer being deposited by the film deposition tool set over the bonding layer.

23. A manufacturing tool configuration as claimed in claim 15 wherein the film deposition tool set deposits a substantially planar bonding layer directly on the dielectric layer.

24. A manufacturing tool configuration as claimed in claim 15 wherein the pattern processing tool set is a photoresist processing tool set.

25. A manufacturing tool configuration as claimed in claim 15 wherein the dielectric deposition tool set deposits a low-K dielectric material.

26. A manufacturing tool configuration as claimed in claim 15 wherein the film deposition tool set is a single integrated tool.

27. A manufacturing tool configuration as claimed in claim 15 wherein the pattern processing tool set is a single integrated tool.

28. A manufacturing tool configuration as claimed in claim 15 wherein the dielectric deposition tool set is a single integrated tool.

29. A manufacturing tool configuration as claimed in claim 15 wherein the inspection tool set inspects the workpiece to ensure proper registration of the interconnect line pattern and the post pattern formed by the pattern processing tool set.

30. A manufacturing tool configuration as claimed in claim 15 wherein the inspection tool set inspects the workpiece to ensure proper dielectric etching by the dielectric processing tool set.

31. A manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

a film deposition tool set for depositing a barrier layer exterior to the planar dielectric surface and for depositing a seed layer exterior to the barrier layer;

a pattern processing tool set for providing an interconnect line pattern over the seed layer and for providing a post pattern over interconnect line metallization formed using the interconnect line pattern;

a wet processing tool set for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition

process, into the interconnect line pattern and the post pattern formed by the pattern processing tool set,

removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern,

removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization; and

a dielectric processing tool set for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using no more than five workpiece movements between the tool sets.

32. A manufacturing tool configuration as claimed in claim 30 wherein the wet processing tool set comprises at least one processing station for applying an electrochemically deposited protective coating exterior to the copper metallization.

33. A manufacturing tool configuration as claimed in claim 31 wherein the wet processing tool set comprises at least one processing station for conditioning

a surface of the workpiece prior to further processing within the wet processing tool set.

34. A manufacturing tool configuration as claimed in claim 31 wherein the wet processing tool set comprises at least one processing station for oxidizing exposed metallized portions of the workpiece.

35. A manufacturing tool configuration as claimed in claim 34 wherein the wet processing tool set comprises at least one processing station for removing the oxidized metal portions of the workpiece.

36. A manufacturing tool configuration as claimed in claim 35 wherein the at least one processing station for removing oxidized metal portions is also employed for conditioning of surfaces prior to subsequent processing.

37. A manufacturing tool configuration as claimed in claim 31 wherein the film deposition tool set is a vacuum deposition tool set.

38. A manufacturing tool configuration as claimed in claim 31 wherein the film deposition tool set deposits a substantially planar bonding layer, the barrier layer being deposited by the film deposition tool set over the bonding layer.

39. A manufacturing tool configuration as claimed in claim 31 wherein the film deposition tool set deposits a substantially planar bonding layer directly on the dielectric layer.

40. A manufacturing tool configuration as claimed in claim 31 wherein the pattern processing tool set is a photoresist processing tool set.

41. A manufacturing tool configuration as claimed in claim 31 wherein the dielectric deposition tool set deposits a low-K dielectric material.

42. A manufacturing tool configuration as claimed in claim 31 wherein the film deposition tool set is a single integrated tool.

43. A manufacturing tool configuration as claimed in claim 31 wherein the pattern processing tool set is a single integrated tool.

44. A manufacturing tool configuration as claimed in claim 31 wherein the dielectric deposition tool set is a single integrated tool.

45. A manufacturing configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

first means for depositing a barrier layer exterior to the planar dielectric surface and for depositing a seed layer exterior to the barrier layer;

second means for providing an interconnect line pattern over the seed layer and for providing a post pattern over interconnect line metallization formed using the interconnect line pattern;

third means for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed by the second means,

removing material applied by the second means to form the interconnect line pattern and the post pattern,

removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization; and

fourth means for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using no more

than ten workpiece movements between the first, second, third, and fourth means.

46. A manufacturing configuration as claimed in claim 45 wherein the third means comprises means for applying an electrochemically deposited protective coating exterior to the copper metallization.

47. A manufacturing configuration as claimed in claim 45 wherein the third means comprises at least one processing station for conditioning a surface of the workpiece prior to further processing by the third means.

48. A manufacturing configuration as claimed in claim 45 wherein the third means comprises at least one processing station for oxidizing exposed metallized portions of the workpiece.

49. A manufacturing configuration as claimed in claim 48 wherein the third means comprises at least one processing station for removing oxidized metal portions of the workpiece.

50. A manufacturing tool configuration as claimed in claim 49 wherein the at least one processing station for removing oxidized metal portions is also employed for conditioning of surfaces prior to subsequent processing.

51. A manufacturing configuration as claimed in claim 45 wherein the single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric is formed using no more than five workpiece movements between the first, second, third, and fourth means.

52. A manufacturing configuration as claimed in claim 45 wherein the first means is a vacuum deposition tool set.

53. A manufacturing configuration as claimed in claim 45 wherein the first means deposits a substantially planar bonding layer, the barrier layer being deposited by the first means over the bonding layer.

54. A manufacturing configuration as claimed in claim 45 wherein the first means deposits a substantially planar bonding layer directly on the dielectric layer.

55. A manufacturing configuration as claimed in claim 45 wherein the second means is a photoresist processing tool set.

56. A manufacturing configuration as claimed in claim 45 wherein the fourth means deposits a low-K dielectric material.

57. A manufacturing configuration as claimed in claim 45 and further comprising fifth means for inspecting the workpiece at one or more processing states during formation of a single metallization level.

58. A manufacturing configuration as claimed in claim 51 wherein the first means is a vacuum deposition tool set.

59. A manufacturing configuration as claimed in claim 51 wherein the first means deposits a substantially planar bonding layer, the barrier layer being deposited by the first means over the bonding layer.

60. A manufacturing configuration as claimed in claim 51 wherein the film deposition tool set deposits a substantially planar bonding layer directly on the dielectric layer.

61. A manufacturing configuration as claimed in claim 51 wherein the second means is a photoresist processing tool set.

62. A manufacturing configuration as claimed in claim 51 wherein the fourth means deposits a low-K dielectric material.

63. A manufacturing configuration as claimed in claim 51 and further comprising fifth means for inspecting the workpiece at one or more processing states during formation of a single metallization level.

64. A manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

a film deposition tool set for depositing a barrier layer exterior to the planar dielectric surface;

a pattern processing tool set for providing an interconnect line pattern exterior to the barrier layer and for providing a post pattern over interconnect line metallization formed using the interconnect line pattern;

a wet processing tool set for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed by the pattern processing tool set,

removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern,

removing portions of the barrier layer that are not overlied by interconnect line metallization; and

a dielectric processing tool set for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using no more than ten workpiece movements between the tool sets.

65. A processing toll architecture as claimed in claim 64 wherein the single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer is formed using no more than five workpiece movements between the tool sets.

66. A manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

a film deposition tool set for depositing a barrier layer exterior to the planar dielectric surface and for depositing a seed layer exterior to the barrier layer;

a pattern processing tool set for providing an interconnect line pattern over the seed layer and for providing a post pattern over interconnect line metallization formed using the interconnect line pattern;

a wet processing tool set for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed by the pattern processing tool set,

removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern,

removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization; and

a dielectric processing tool set for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using a plurality of workpiece movements between the tool sets.

67. A process for providing one or more protected copper elements on a surface of a workpiece, the process comprising the steps of:

applying a barrier layer to the workpiece;

applying a seed layer on the barrier layer;

electroplating one or more copper elements on selected portions of the seed layer;

substantially removing the seed layer;

rendering at least a portion of a surface of the barrier layer unplatable; and

electroplating a protective layer onto surfaces of the one or more copper elements.

68. A process as claimed in claim 67 and further comprising the step of applying a dielectric layer over at least a portion of the one or more copper elements.

69. A process as claimed in claim 67 wherein the step of substantially removing the seed layer comprises the step of subjecting the seed layer to an electrolyte solution bath containing phosphoric acid while holding the seed layer at a positive electrical potential relative to an electrode that is immersed in the electrolyte solution bath.

70. A process as claimed in claim 67 and further comprising the steps of:

applying a dielectric layer to substantially cover the one or more copper elements;

removing a surface portion of the dielectric layer to expose one or more upper regions of the one or more copper elements.

71. A process as claimed in claim 67 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the step of oxidizing exposed surfaces of the barrier layer material.

72. A process as claimed in claim 67 wherein the step of electroplating one or more copper elements on selected portions of the seed layer comprises the steps of:

electroplating one or more copper lines on selected portions of the seed layer; and

electroplating one or more copper posts on selective portions of the copper lines.

73. A process as claimed in claim 67 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the steps of :

concurrently oxidizing exposed surfaces of the barrier layer material and the one or more copper elements;

removing the resultant copper oxide from the one or more copper elements.

74. A process as claimed in claim 73 wherein the step of substantially removing the seed layer concurrently occurs during the step of removing resultant copper oxide layers from the one or more copper elements.

75. A process as claimed in claim 73 wherein the step of electroplating one or more copper elements on selected portions of the seed layer comprises the steps of:

electroplating one or more copper lines on selected portions of the seed layer; and

electroplating one or more copper posts on selective portions of the copper lines.

76. A process as claimed in claim 67 and further comprising the step of removing the barrier layer after electroplating the protective layer.

77. A process as claimed in claim 67 wherein the barrier layer and seed layer are applied in a first processing tool set.

78. A process as claimed in claim 77 wherein the wherein the electroplating steps and the rendering step are executed in a second processing tool set.

79. A process as claimed in claim 78 wherein the first processing tool set is a vacuum deposition tool set.

80. A process as claimed in claim 79 wherein the second processing tool set is a wet processing tool set.

81. A process as claimed in claim 77 wherein the first processing tool set is a vacuum deposition tool set.

82. A process as claimed in claim 67 wherein the barrier layer is comprised of tantalum.

83. A process as claimed in claim 67 wherein the seed layer is comprised of copper.

84. A process as claimed in claim 67 wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

85. A process as claimed in claim 67 wherein the step of electroplating one or more copper elements is comprised of the steps of:

applying a pattern mask layer over the seed layer whereby the selected portions of the seed layer are exposed; and

electroplating the one or more copper elements onto the seed layer through the exposed selected portions.

86. A process for providing one or more protected copper elements on a surface of a workpiece, the process comprising the steps of:

applying a conductive barrier layer to the workpiece;

electroplating one or more copper elements on selected portions of the conductive barrier layer;

rendering at least a portion of a surface of the conductive barrier layer unplatable; and

electroplating a protective layer onto surfaces of the one or more copper elements.

87. A process as claimed in claim 86 and further comprising the step of applying a dielectric layer over at least a portion of the one or more copper elements.

88. A process as claimed in claim 86 and further comprising the steps of:

applying a dielectric layer to substantially cover the one or more copper elements;

removing a surface portion of the dielectric layer to expose one or more upper regions of the one or more copper elements.

89. A process as claimed in claim 86 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the step of oxidizing exposed surfaces of the barrier layer material.

90. A process as claimed in claim 86 wherein the step of electroplating one or more copper elements on selected portions of the conductive barrier layer comprises the steps of:

electroplating one or more copper lines on selected portions of the conductive barrier layer; and

electroplating one or more copper posts on selective portions of the copper lines.

91. A process as claimed in claim 86 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the steps of:

concurrently oxidizing exposed surfaces of the barrier layer material and the one or more copper elements;

removing the resultant copper oxide from the one or more copper elements.

92. A process as claimed in claim 86 and further comprising the step of removing the barrier layer after electroplating the protective layer.

93. A process as claimed in claim 86 wherein the barrier layer is applied in a first processing tool set.

94. A process as claimed in claim 93 wherein the wherein the electroplating steps and the rendering step are executed in a second processing tool set.

95. A process as claimed in claim 94 wherein the first processing tool set is a vacuum deposition tool set.

96. A process as claimed in claim 95 wherein the second processing tool set is a wet processing tool set.

97. A process as claimed in claim 93 wherein the first processing tool set is a vacuum deposition tool set.

98. A process as claimed in claim 86 wherein the barrier layer is comprised of titanium nitride.

99. A process as claimed in claim 86 wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

100. A process as claimed in claim 86 wherein the barrier layer comprises titanium nitride overlying tantalum nitride and wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

101. A process as claimed in claim 86 wherein the step of electroplating one or more copper elements is comprised of the steps of:

applying a pattern mask layer over the barrier layer whereby the selected portions of the conductive barrier layer are exposed; and

electroplating the one or more copper elements onto the conductive barrier layer through the exposed selected portions.

102. A process for providing one or more copper metallization layers on a surface of a semiconductor workpiece, the process comprising the steps of:

applying a barrier layer to the semiconductor workpiece;

applying a seed layer on the barrier layer;

electroplating one or more copper interconnect lines on selected portions of the seed layer;

electroplating one or more copper posts on selected portions of the copper interconnect lines;

substantially removing the seed layer;

concurrently oxidizing exposed surfaces of the one or more copper interconnect lines, exposed surfaces of the one or more copper posts, and exposed surfaces of the barrier layer;

removing resultant copper oxide layers from the one or more copper interconnect lines and the one or more copper posts while leaving the oxidized barrier

layer surfaces substantially intact so as to leave the barrier layer surfaces unplatable;

electroplating a protective layer onto exposed surfaces of the one or more copper interconnect lines.

103. A process as claimed in claim 102 and further comprising the step of applying a dielectric layer over at least a portion of the one or more copper elements.

104. A process as claimed in claim 102 and further comprising the steps of:

applying a dielectric layer to substantially cover the one or more copper interconnect lines and the one or more copper posts;

removing a surface portion of the dielectric layer to expose upper regions of the one or more copper posts.

105. A process as claimed in claim 102 and further comprising the step of removing the barrier layer after electroplating the protective layer.

106. A process as claimed in claim 102 wherein the barrier layer and seed layer are applied in a first processing tool set.

107. A process as claimed in claim 106 wherein the wherein the electroplating steps and the oxidizing step are executed in a second processing tool set.

108. A process as claimed in claim 107 wherein the first processing tool set is a vacuum deposition tool set.

109. A process as claimed in claim 108 wherein the second processing tool set is a wet processing tool set.

110. A process as claimed in claim 106 wherein the first processing tool set is a vacuum deposition tool set.

111. A process as claimed in claim 102 wherein the step of electroplating one or more copper interconnect lines is comprised of the steps of:

applying a pattern mask layer over the seed layer whereby the selected portions of the seed layer are exposed; and

electroplating the one or more copper interconnect lines onto the seed layer through the exposed selected portions.

112. A process as claimed in claim 111 wherein the step of electroplating one or more copper posts is comprised of the steps of:

applying a pattern mask layer over the seed layer and the one or more interconnect lines whereby selected upper portions of the copper interconnect lines are exposed; and

electroplating the one or more copper posts onto the copper interconnects lines through the exposed portions.

113. A process as claimed in claim 102 wherein the barrier layer is comprised of tantalum.

114. A process as claimed in claim 102 wherein the seed layer is comprised of copper.

115. A process as claimed in claim 102 wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

116. A process as claimed in claim 102 wherein the step of substantially removing the seed layer concurrently occurs during the step of removing resultant copper oxide layers from the one or more copper interconnect lines and the one or more copper posts .

117. A process as claimed in claim 102 wherein the step of substantially removing the seed layer comprises the step of subjecting the seed layer to an electrolyte solution bath containing phosphoric acid while holding the seed layer at a positive electrical potential relative to an electrode that is immersed in the electrolyte solution bath.

118. A process for providing one or more protected copper elements on a surface of a workpiece, the process comprising the steps of:

applying a barrier layer to the workpiece;

applying a seed layer on the barrier layer;

electroplating one or more copper elements on selected portions of the seed layer;

substantially removing the seed layer;

rendering at least a portion of a surface of the barrier layer unplatable; and

electroplating a protective layer onto surfaces of the one or more copper elements.

119. A process as claimed in claim 118 and further comprising the step of applying a dielectric layer over at least a portion of the one or more copper elements.

120. A process as claimed in claim 118 wherein the step of substantially removing the seed layer comprises the step of subjecting the seed layer to an

electrolyte solution bath containing phosphoric acid while holding the seed layer at a positive electrical potential relative to an electrode that is immersed in the electrolyte solution bath.

121. A process as claimed in claim 118 and further comprising the steps of:

applying a dielectric layer to substantially cover the one or more copper elements;

removing a surface portion of the dielectric layer to expose one or more upper regions of the one or more copper elements.

122. A process as claimed in claim 118 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the step of oxidizing exposed surfaces of the barrier layer material.

123. A process as claimed in claim 118 wherein the step of electroplating one or more copper elements on selected portions of the seed layer comprises the steps of:

electroplating one or more copper lines on selected portions of the seed layer; and

electroplating one or more copper posts on selective portions of the copper lines.

124. A process as claimed in claim 118 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the steps of :

concurrently oxidizing exposed surfaces of the barrier layer material and the one or more copper elements;

removing the resultant copper oxide from the one or more copper elements.

125. A process as claimed in claim 124 wherein the step of substantially removing the seed layer concurrently occurs during the step of removing resultant copper oxide layers from the one or more copper elements.

126. A process as claimed in claim 124 wherein the step of electroplating one or more copper elements on selected portions of the seed layer comprises the steps of:

electroplating one or more copper lines on selected portions of the seed layer; and

electroplating one or more copper posts on selective portions of the copper lines.

127. A process as claimed in claim 118 and further comprising the step of removing the barrier layer after electroplating the protective layer.

128. A process as claimed in claim 118 wherein the barrier layer and seed layer are applied in a first processing tool set.

129. A process as claimed in claim 128 wherein the wherein the electroplating steps and the rendering step are executed in a second processing tool set.

130. A process as claimed in claim 129 wherein the first processing tool set is a vacuum deposition tool set.

131. A process as claimed in claim 130 wherein the second processing tool set is a wet processing tool set.

132. A process as claimed in claim 128 wherein the first processing tool set is a vacuum deposition tool set.

133. A process as claimed in claim 118 wherein the barrier layer is comprised of tantalum.

134. A process as claimed in claim 118 wherein the seed layer is comprised of copper.

135. A process as claimed in claim 118 wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

136. A process as claimed in claim 118 wherein the step of electroplating one or more copper elements is comprised of the steps of:

applying a pattern mask layer over the seed layer whereby the selected portions of the seed layer are exposed; and

electroplating the one or more copper elements onto the seed layer through the exposed selected portions.

137. A process for providing one or more protected copper elements on a surface of a workpiece, the process comprising the steps of:

applying a conductive barrier layer to the workpiece;

electroplating one or more copper elements on selected portions of the conductive barrier layer;

rendering at least a portion of a surface of the conductive barrier layer unplatable; and

electroplating a protective layer onto surfaces of the one or more copper elements.

138. A process as claimed in claim 137 and further comprising the step of applying a dielectric layer over at least a portion of the one or more copper elements.

139. A process as claimed in claim 137 and further comprising the steps of:

applying a dielectric layer to substantially cover the one or more copper elements;

removing a surface portion of the dielectric layer to expose one or more upper regions of the one or more copper elements.

140. A process as claimed in claim 137 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the step of oxidizing exposed surfaces of the barrier layer material.

141. A process as claimed in claim 137 wherein the step of electroplating one or more copper elements on selected portions of the conductive barrier layer comprises the steps of:

electroplating one or more copper lines on selected portions of the conductive barrier layer; and

electroplating one or more copper posts on selective portions of the copper lines.

142. A process as claimed in claim 137 wherein the step of rendering at least a portion of a surface of the barrier layer unplatable comprises the steps of :

concurrently oxidizing exposed surfaces of the barrier layer material and the one or more copper elements;

removing the resultant copper oxide from the one or more copper elements.

143. A process as claimed in claim 137 and further comprising the step of removing the barrier layer after electroplating the protective layer.

144. A process as claimed in claim 137 wherein the barrier layer is applied in a first processing tool set.

145. A process as claimed in claim 144 wherein the wherein the electroplating steps and the rendering step are executed in a second processing tool set.

146. A process as claimed in claim 145 wherein the first processing tool set is a vacuum deposition tool set.

147. A process as claimed in claim 146 wherein the second processing tool set is a wet processing tool set.

148. A process as claimed in claim 144 wherein the first processing tool set is a vacuum deposition tool set.

149. A process as claimed in claim 137 wherein the barrier layer is comprised of titanium nitride.

150. A process as claimed in claim 137 wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

151. A process as claimed in claim 137 wherein the barrier layer comprises titanium nitride overlying tantalum nitride and wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

152. A process as claimed in claim 137 wherein the step of electroplating one or more copper elements is comprised of the steps of:

applying a pattern mask layer over the barrier layer whereby the selected portions of the conductive barrier layer are exposed; and

electroplating the one or more copper elements onto the conductive barrier layer through the exposed selected portions.

153. A process for providing one or more copper metallization layers on a surface of a semiconductor workpiece, the process comprising the steps of:

applying a barrier layer to the semiconductor workpiece;

applying a seed layer on the barrier layer;

electroplating one or more copper interconnect lines on selected portions of the seed layer;

electroplating one or more copper posts on selected portions of the copper interconnect lines;

substantially removing the seed layer;

concurrently oxidizing exposed surfaces of the one or more copper interconnect lines, exposed surfaces of the one or more copper posts, and exposed surfaces of the barrier layer;

removing resultant copper oxide layers from the one or more copper interconnect lines and the one or more copper posts while leaving the oxidized barrier layer surfaces substantially intact so as to leave the barrier layer surfaces unplatable;

electroplating a protective layer onto exposed surfaces of the one or more copper interconnect lines.

154. A process as claimed in claim 153 and further comprising the step of applying a dielectric layer over at least a portion of the one or more copper elements.

155. A process as claimed in claim 153 and further comprising the steps of:

applying a dielectric layer to substantially cover the one or more copper interconnect lines and the one or more copper posts;

removing a surface portion of the dielectric layer to expose upper regions of the one or more copper posts.

156. A process as claimed in claim 153 and further comprising the step of removing the barrier layer after electroplating the protective layer.

157. A process as claimed in claim 153 wherein the step of electroplating one or more copper interconnect lines is comprised of the steps of:

applying a pattern mask layer over the seed layer whereby the selected portions of the seed layer are exposed; and

electroplating the one or more copper interconnect lines onto the seed layer through the exposed selected portions.

158. A process as claimed in claim 153 wherein the step of electroplating one or more copper posts is comprised of the steps of:

applying a pattern mask layer over the seed layer and the one or more interconnect lines whereby selected upper portions of the copper interconnect lines are exposed; and

electroplating the one or more copper posts onto the copper interconnects lines through the exposed portions.

159. A process as claimed in claim 153 wherein the barrier layer is comprised of tantalum.

160. A process as claimed in claim 153 wherein the seed layer is comprised of copper.

161. A process as claimed in claim 153 wherein the protective layer is comprised of a material selected from the group consisting of nickel, nickel alloys, and chromium.

162. A process as claimed in claim 153 wherein the step of substantially removing the seed layer concurrently occurs during the step of removing resultant copper oxide layers from the one or more copper interconnect lines and the one or more copper posts .

163. A process as claimed in claim 153 wherein the step of substantially removing the seed layer comprises the step of subjecting the seed layer to an electrolyte solution bath containing phosphoric acid while holding the seed layer at a positive electrical potential relative to an electrode that is immersed in the electrolyte solution bath.

164. A manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

a film deposition tool set for depositing a barrier layer exterior to the planar dielectric surface and for depositing a seed layer exterior to the barrier layer;

a hard mask formation tool set for forming a hard mask dielectric layer exterior to the seed layer;

a pattern processing tool set for providing an interconnect line pattern over the hard mask dielectric layer and for providing a post pattern over interconnect line metallization formed using the interconnect line pattern;

a hard mask etching tool set for etching exposed regions of the hard mask dielectric layer after formation of the interconnect line pattern thereover;

a wet processing tool set for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern defined in the hard mask and the post pattern defined by the pattern material used by the pattern processing tool set,

removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern,

removing the hard mask dielectric layer,

removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization; and

a dielectric processing tool set for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using no more than twelve workpiece movements between the tool sets.

165. A manufacturing tool configuration as claimed in claim 164 wherein the wet processing tool set comprises at least one processing station for applying an electrochemically deposited protective coating exterior to the copper metallization.

166. A manufacturing tool configuration as claimed in claim 164 wherein the wet processing tool set comprises at least one processing station for conditioning a surface of the workpiece prior to further processing within the wet processing tool set.

167. A manufacturing tool configuration as claimed in claim 164 wherein the wet processing tool set comprises at least one processing station for oxidizing exposed metallized portions of the workpiece.

168. A manufacturing tool configuration as claimed in claim 167 wherein the wet processing tool set comprises at least one processing station for removing oxidized metal portions of the workpiece.

169. A manufacturing tool configuration as claimed in claim 168 wherein the at least one processing station for removing oxidized metal portions is also employed for conditioning of surfaces prior to subsequent processing.

170. A manufacturing tool configuration as claimed in claim 164 wherein the film deposition tool set is a vacuum deposition tool set.

171. A manufacturing tool configuration as claimed in claim 164 wherein the film deposition tool set deposits a substantially planar bonding layer, the barrier layer being deposited by the film deposition tool set over the bonding layer.

172. A manufacturing tool configuration as claimed in claim 164 wherein the film deposition tool set deposits a substantially planar bonding layer directly on the dielectric layer.

173. A manufacturing tool configuration as claimed in claim 164 wherein the pattern processing tool set is a photoresist processing tool set.

174. A manufacturing tool configuration as claimed in claim 164 wherein the dielectric deposition tool set deposits a low-K dielectric material.

175. A manufacturing tool configuration as claimed in claim 164 wherein the film deposition tool set is a single integrated tool.

176. A manufacturing tool configuration as claimed in claim 164 wherein the pattern processing tool set is a single integrated tool.

177. A manufacturing tool configuration as claimed in claim 164 wherein the dielectric deposition tool set is a single integrated tool.

178. A manufacturing tool configuration as claimed in claim 164 wherein the electrochemical/wet processing tool set is a single integrated tool.

179. A manufacturing tool configuration as claimed in claim 164 and further comprising an inspection tool set for inspecting the workpiece at one or more processing states during formation of a single metallization level.

180. A manufacturing tool configuration as claimed in claim 179 wherein the wet processing tool set comprises at least one processing station for applying

an electrochemically deposited protective coating exterior to the copper metallization.

181. A manufacturing tool configuration as claimed in claim 179 wherein the wet processing tool set comprises at least one processing station for conditioning a surface of the workpiece prior to further processing within the wet processing tool set.

182. A manufacturing tool configuration as claimed in claim 179 wherein the wet processing tool set comprises at least one processing station for oxidizing exposed metallized portions of the workpiece.

183. A manufacturing tool configuration as claimed in claim 182 wherein the wet processing tool set comprises at least one processing station for removing oxidized metal portions of the workpiece.

184. A manufacturing tool configuration as claimed in claim 183 wherein the at least one processing station for oxidizing and the at least one processing station for removing oxidized metal portions are the same processing station.

185. A manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

a film deposition tool set for depositing a barrier layer exterior to the planar dielectric surface and for depositing a seed layer exterior to the barrier layer;

a hard mask formation tool set for forming a hard mask dielectric layer exterior to the seed layer;

a pattern processing tool set for providing an interconnect line pattern over the hard mask dielectric layer and for providing a post pattern over interconnect line metallization formed using the interconnect line pattern;

a hard mask etching tool set for etching exposed regions of the hard mask dielectric layer after formation of the interconnect line pattern thereover;

a wet processing tool set for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern and the post pattern formed using the pattern processing tool set,

removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern,

removing the hard mask dielectric layer,

removing portions of the seed layer and the barrier layer that are

not overlied by interconnect line metallization; and

a dielectric processing tool set for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using no more than seven workpiece movements between the tool sets.

186. A manufacturing tool configuration as claimed in claim 185 wherein the wet processing tool set comprises at least one processing station for applying an electrochemically deposited protective coating exterior to the copper metallization.

187. A manufacturing tool configuration as claimed in claim 185 wherein the wet processing tool set comprises at least one processing station for conditioning a surface of the workpiece prior to further processing within the wet processing tool set.

188. A manufacturing tool configuration as claimed in claim 185 wherein the wet processing tool set comprises at least one processing station for oxidizing exposed metallized portions of the workpiece.

189. A manufacturing tool configuration as claimed in claim 185 wherein the film deposition tool set is a vacuum deposition tool set.

190. A manufacturing tool configuration as claimed in claim 185 wherein the film deposition tool set deposits a substantially planar bonding layer, the barrier layer being deposited by the film deposition tool set over the bonding layer.

191. A manufacturing tool configuration as claimed in claim 185 wherein the film deposition tool set deposits a substantially planar bonding layer directly on the dielectric layer.

192. A manufacturing tool configuration as claimed in claim 185 wherein the pattern processing tool set is a photoresist processing tool set.

193. A manufacturing tool configuration as claimed in claim 185 wherein the dielectric deposition tool set deposits a low-K dielectric material.

194. A manufacturing tool configuration as claimed in claim 185 wherein the film deposition tool set is a single integrated tool.

195. A manufacturing tool configuration as claimed in claim 185 wherein the pattern processing tool set is a single integrated tool.

196. A manufacturing tool configuration as claimed in claim 185 wherein the dielectric deposition tool set is a single integrated tool.

197. A manufacturing tool configuration as claimed in claim 185 wherein the electrochemical/wet processing tool set is a single integrated tool.

198. A manufacturing tool configuration for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a workpiece, the tool configuration comprising:

a film deposition tool set for depositing a barrier layer exterior to the planar dielectric surface and for depositing a seed layer exterior to the barrier layer;

a hard mask formation tool set for forming a first hard mask dielectric layer exterior to the seed layer and for forming a second hard mask dielectric layer exterior to the first hard mask dielectric layer;

a pattern processing tool set for providing an interconnect line pattern over the first hard mask dielectric layer and for providing a post pattern over a second hard mask dielectric layer;

a hard mask etching tool set for etching exposed regions of the first hard mask dielectric layer after formation of the interconnect line pattern thereover and the second hard mask dielectric layer after formation of the post pattern thereover;

a wet processing tool set for performing at least the following wet processing operations,

applying copper metallization, using an electrochemical deposition process, into the interconnect line pattern defined in the first hard mask and into the post pattern defined in the second hard mask,

removing material applied by the pattern processing tool set to form the interconnect line pattern and the post pattern on the hard mask dielectric layers,

removing the hard mask dielectric layers,

removing portions of the seed layer and the barrier layer that are not overlied by interconnect line metallization; and

a dielectric processing tool set for depositing a dielectric layer over the interconnect line metallization and post metallization and for etching the deposited dielectric layer to expose upper connection regions of the post metallization;

a single metallization level comprising the interconnect line metallization, the post metallization, and the dielectric layer being formed using no more than nine workpiece movements between the tool sets.

5

FIG. 1
PRIOR ART

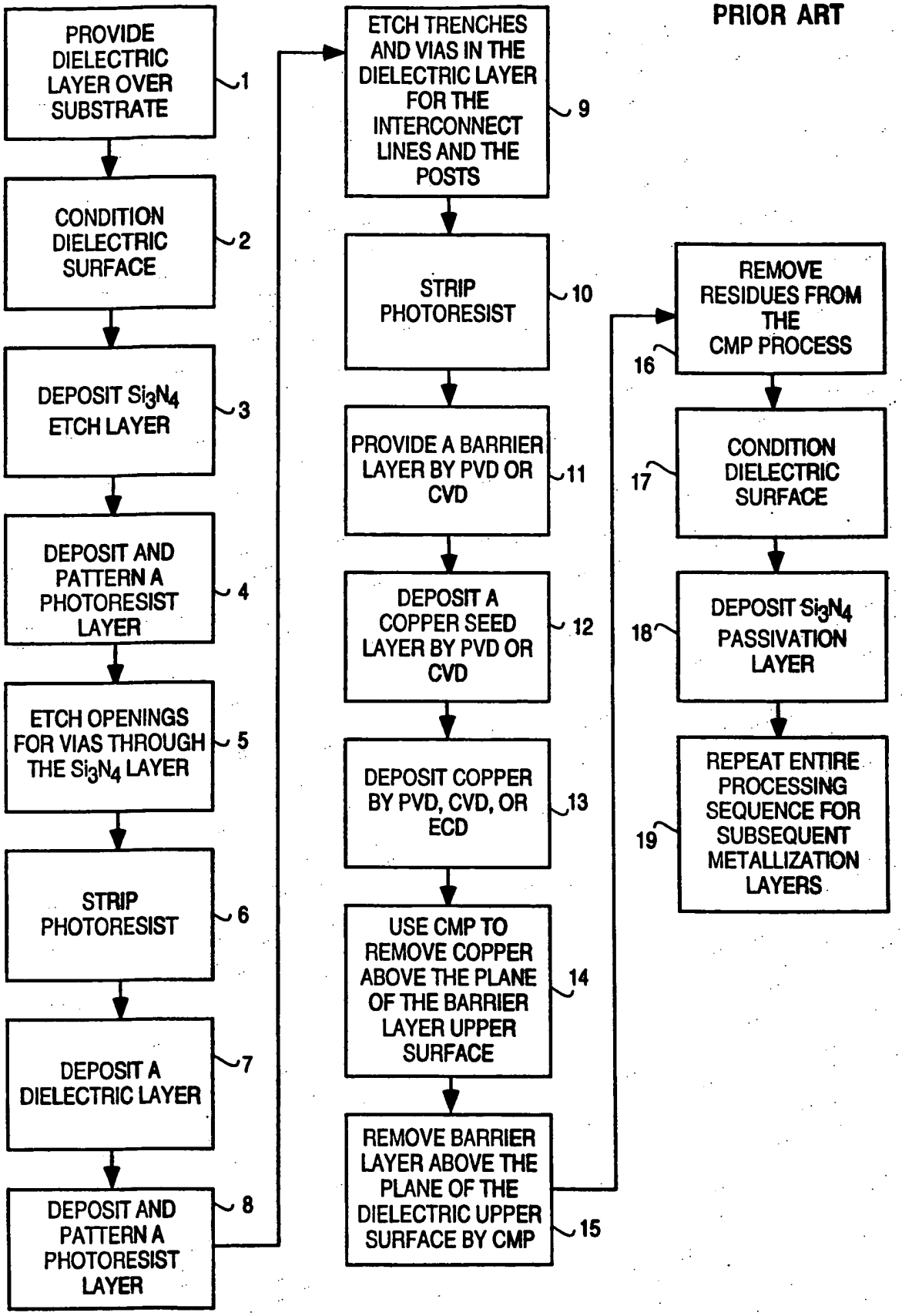


FIG. 2
PRIOR ART

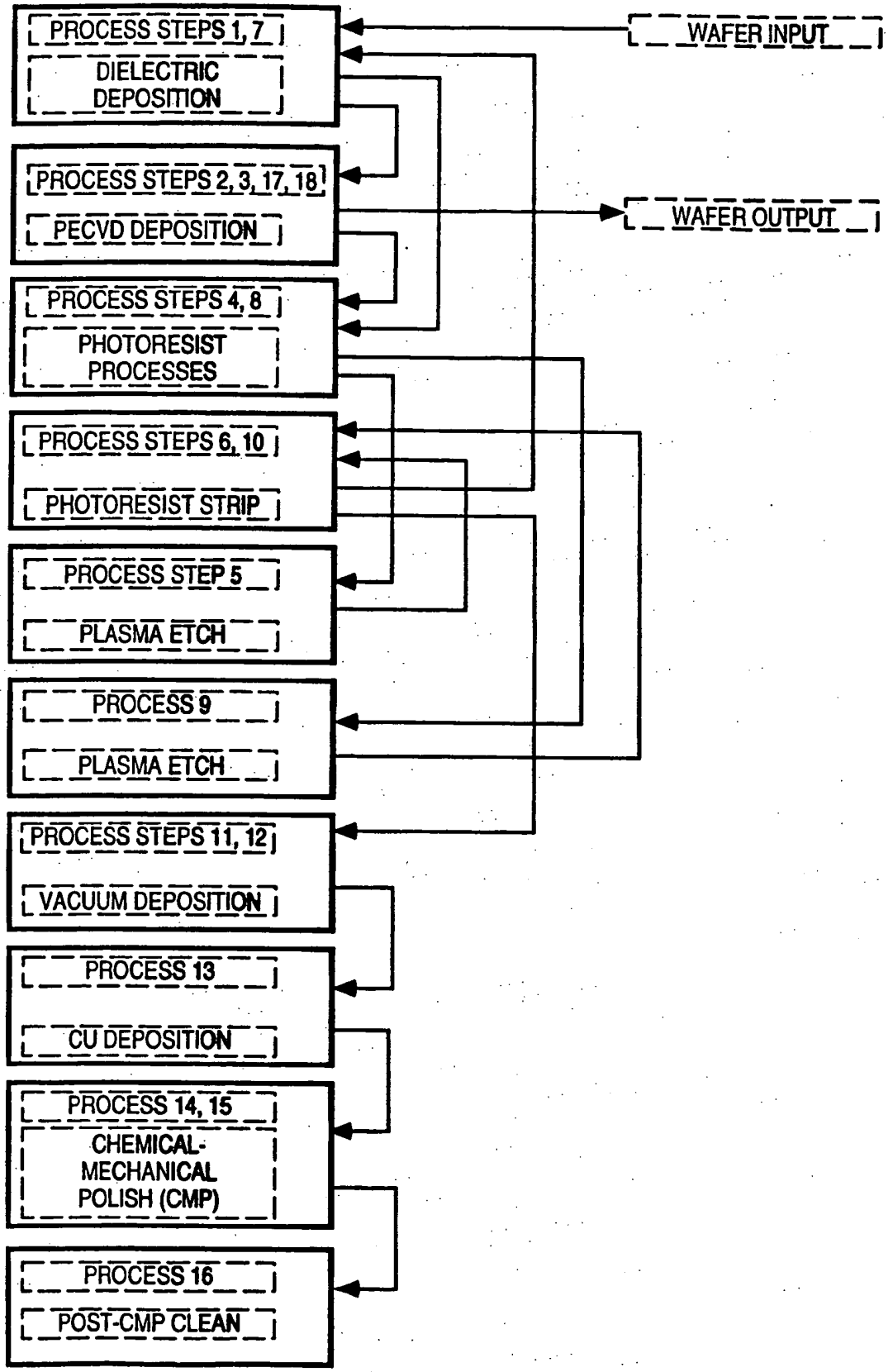


FIG. 3

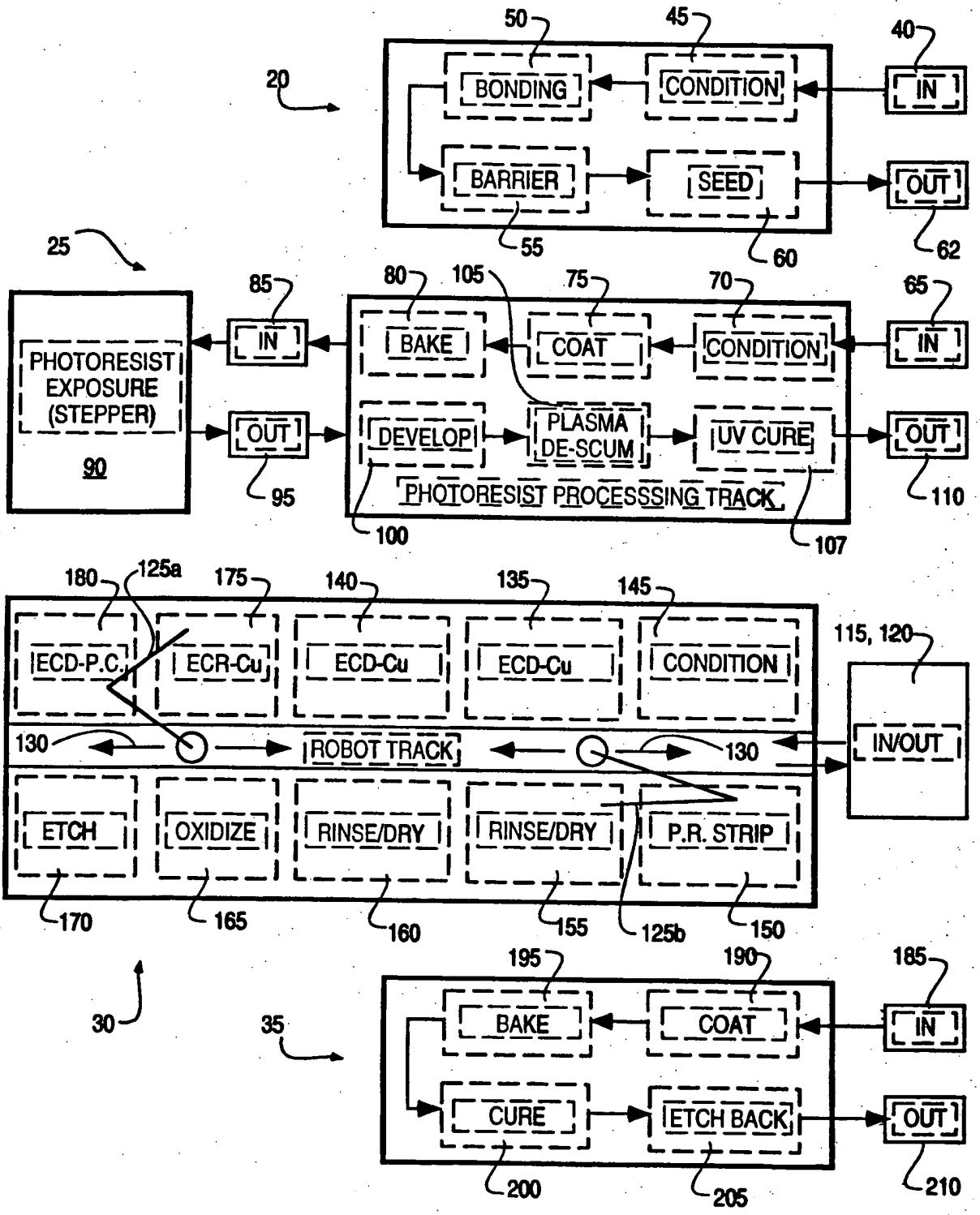

20
50
45
40
BONDING
CONDITION
IN
BARRIER
SEED
OUT
55
60
62
25
85
80
105
75
70
65
PHOTORESIST EXPOSURE (STEPPER)
90
IN
BAKE
COAT
CONDITION
IN
OUT
DEVELOP
PLASMA DE-SCUM
UV CURE
OUT
PHOTORESIST PROCESSSING TRACK
95
100
107
110
180
125a
175
140
135
145
115, 120
ECD-P.C.
ECR-Cu
ECD-Cu
ECD-Cu
CONDITION
130
ROBOT TRACK
130
IN/OUT
ETCH
OXIDIZE
RINSE/DRY
RINSE/DRY
P.R. STRIP
170
165
160
155
125b
150
30
35
195
190
185
BAKE
COAT
IN
CURE
ETCH BACK
OUT
200
205
210

FIG. 4

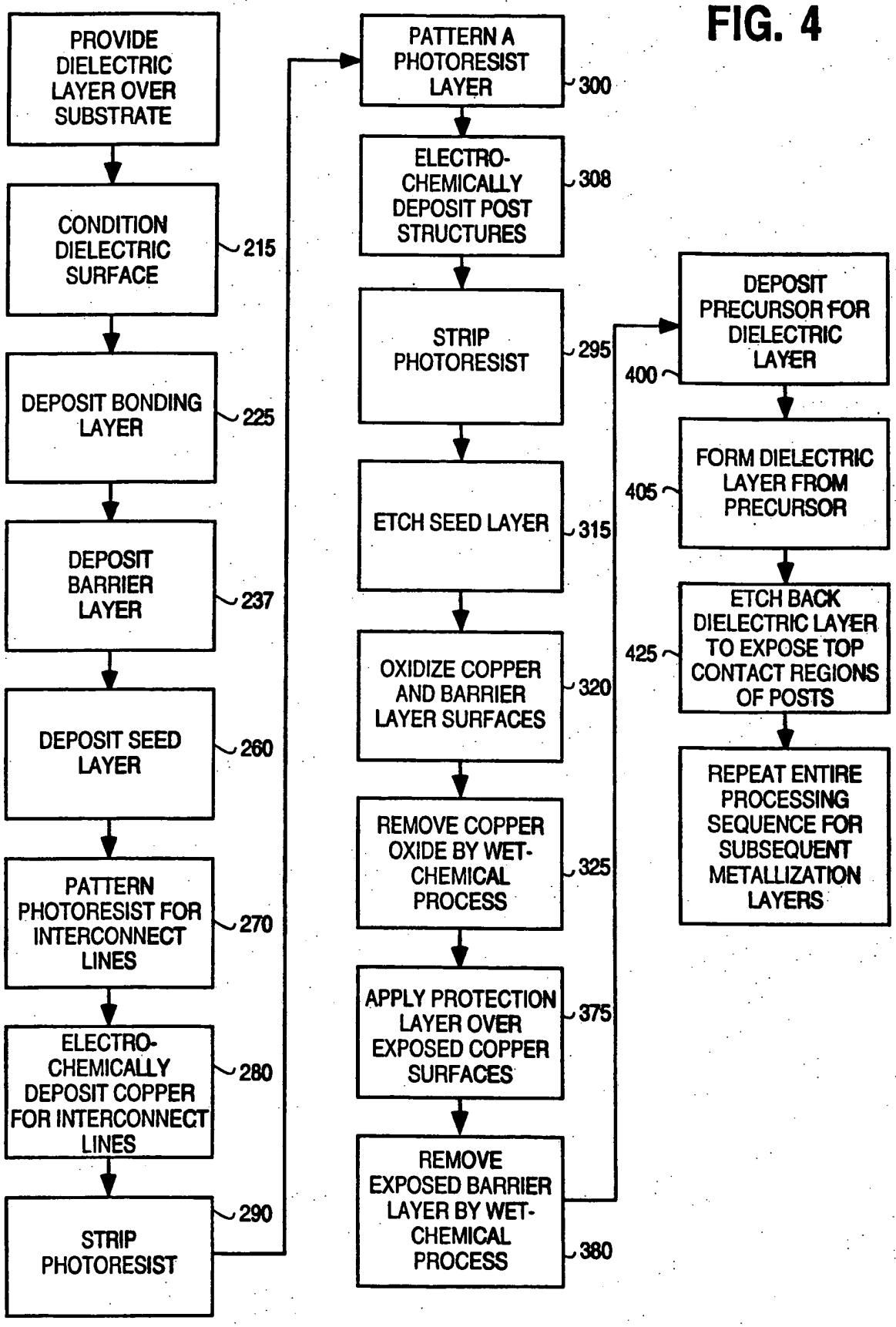

PROVIDE DIELECTRIC LAYER OVER SUBSTRATE
CONDITION DIELECTRIC SURFACE
215
DEPOSIT BONDING LAYER
225
DEPOSIT BARRIER LAYER
237
DEPOSIT SEED LAYER
260
PATTERN PHOTORESIST FOR INTERCONNECT LINES
270
ELECTRO-CHEMICALLY DEPOSIT COPPER FOR INTERCONNECT LINES
280
STRIP PHOTORESIST
290
PATTERN A PHOTORESIST LAYER
300
ELECTRO-CHEMICALLY DEPOSIT POST STRUCTURES
308
STRIP PHOTORESIST
295
ETCH SEED LAYER
315
OXIDIZE COPPER AND BARRIER LAYER SURFACES
320
REMOVE COPPER OXIDE BY WET-CHEMICAL PROCESS
325
APPLY PROTECTION LAYER OVER EXPOSED COPPER SURFACES
375
REMOVE EXPOSED BARRIER LAYER BY WET-CHEMICAL PROCESS
380
DEPOSIT PRECURSOR FOR DIELECTRIC LAYER
400
FORM DIELECTRIC LAYER FROM PRECURSOR
405
ETCH BACK DIELECTRIC LAYER TO EXPOSE TOP CONTACT REGIONS OF POSTS
425
REPEAT ENTIRE PROCESSING SEQUENCE FOR SUBSEQUENT METALLIZATION LAYERS

FIG. 5A

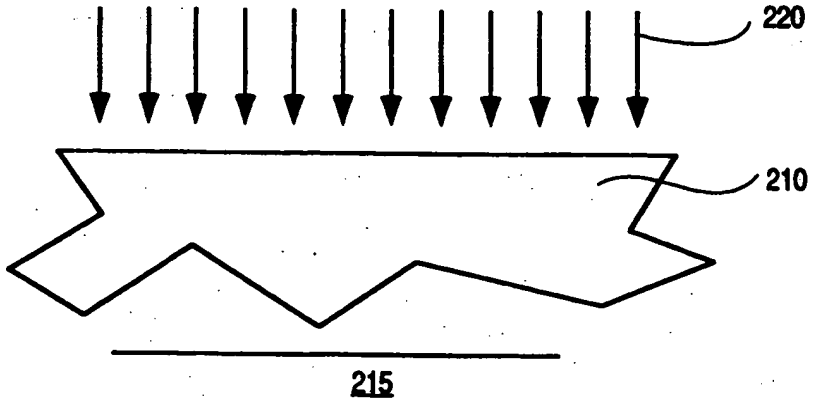


FIG. 5B

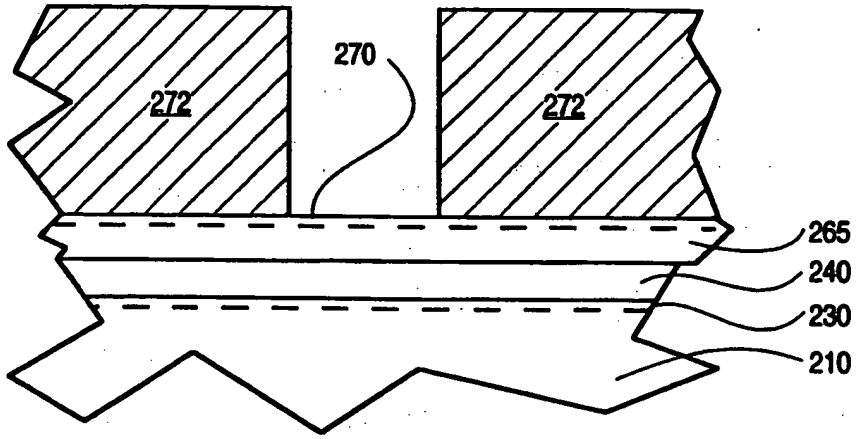


FIG. 5C

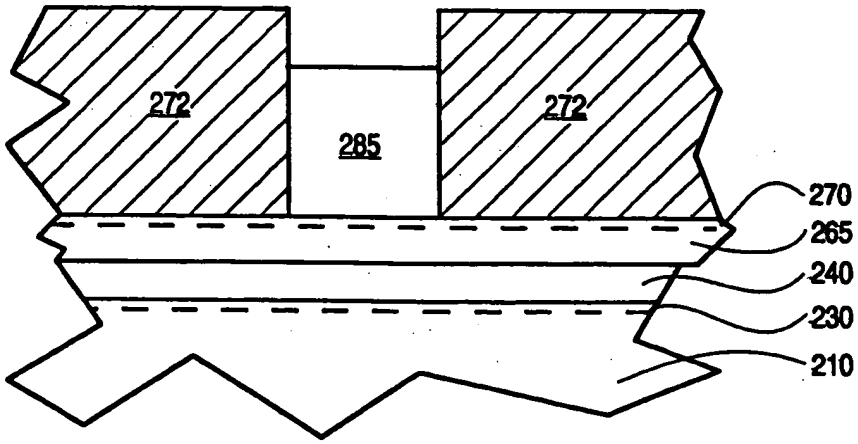


FIG. 5D

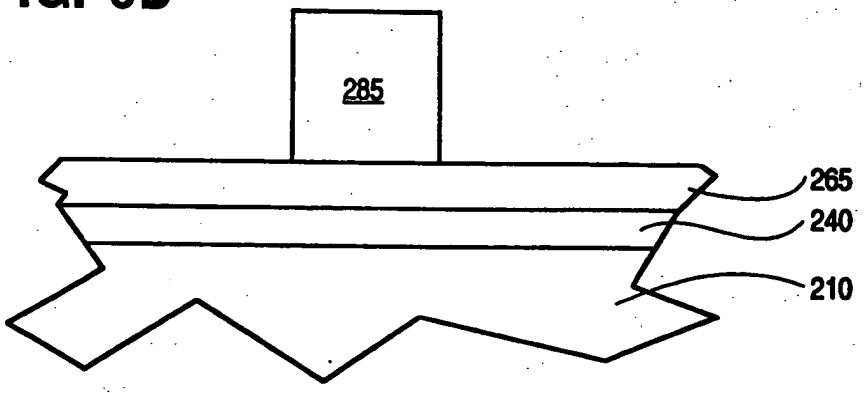


FIG. 5E

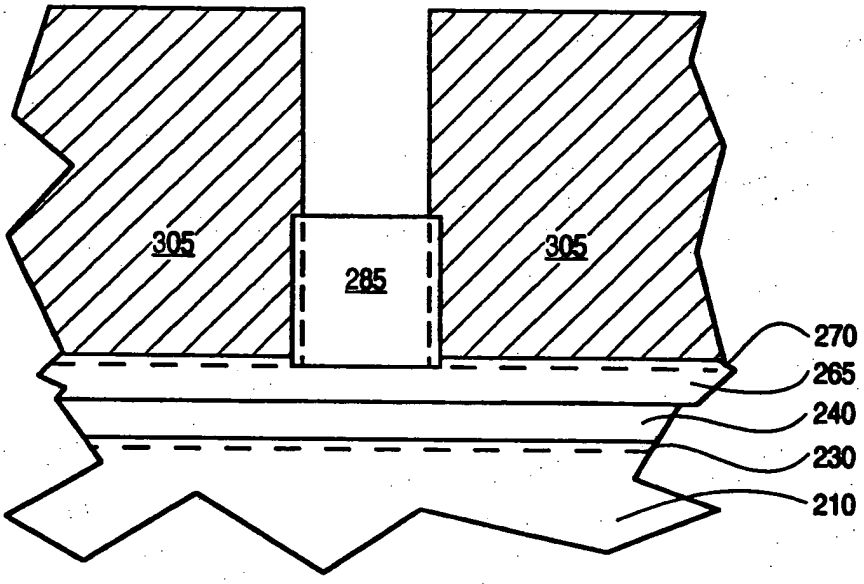


FIG. 5F

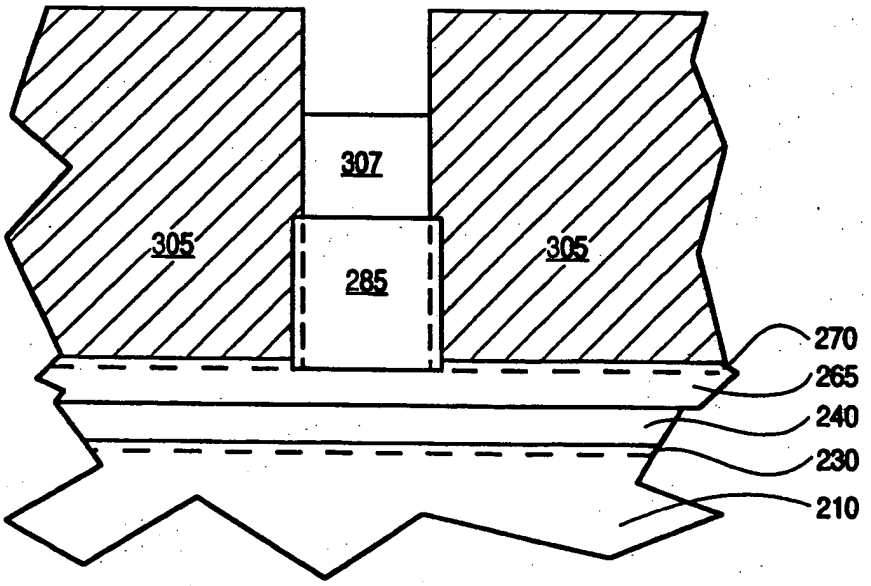


FIG. 5G

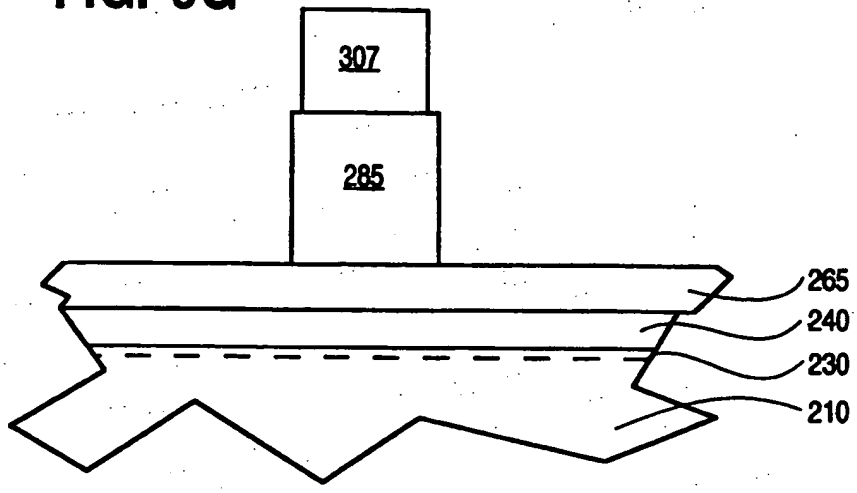


FIG. 5H

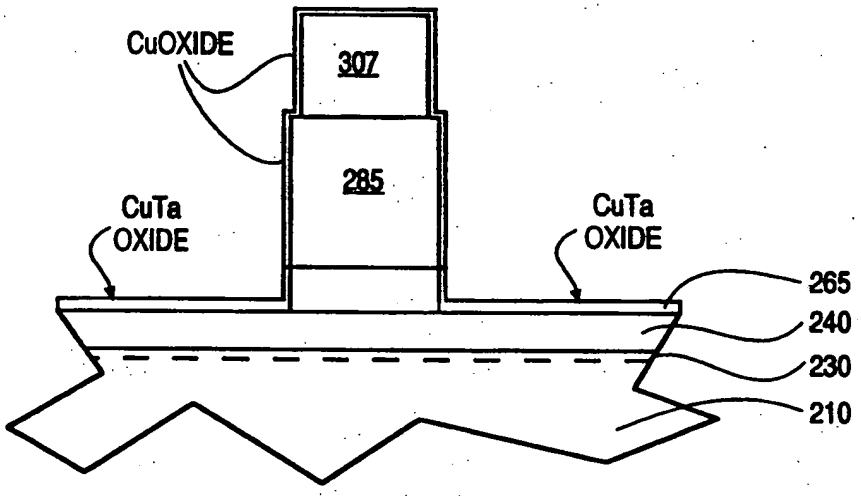


FIG. 5I

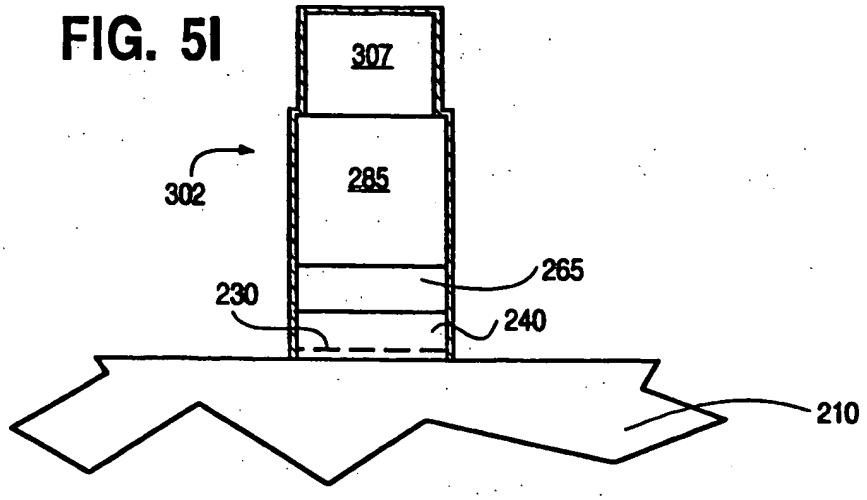


FIG. 5J

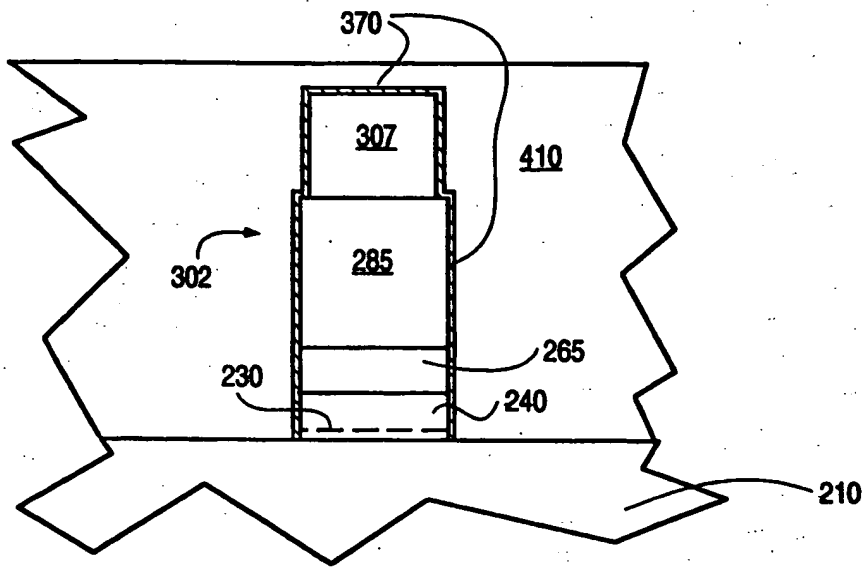

370
307
410
285
302
265
230
240
210

FIG. 5K

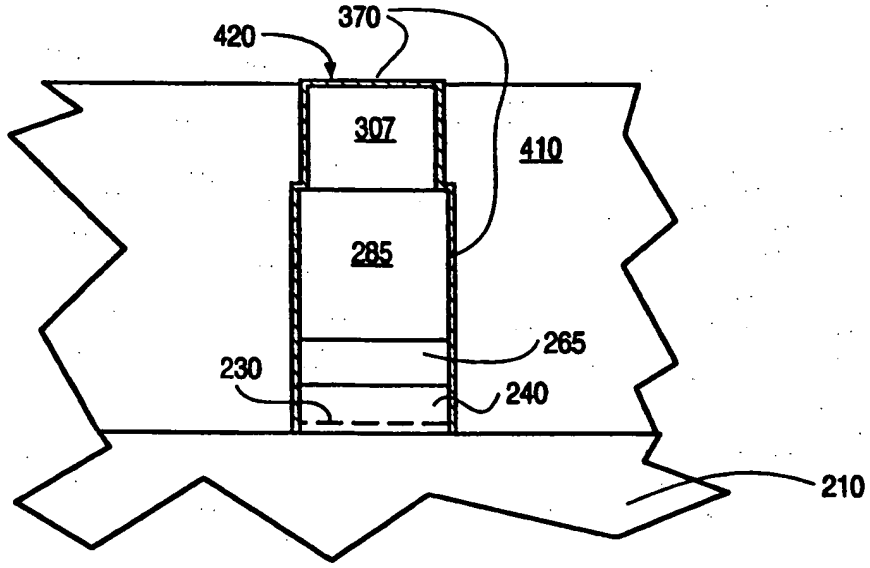

420
370
307
410
285
265
230
240
210

FIG. 6

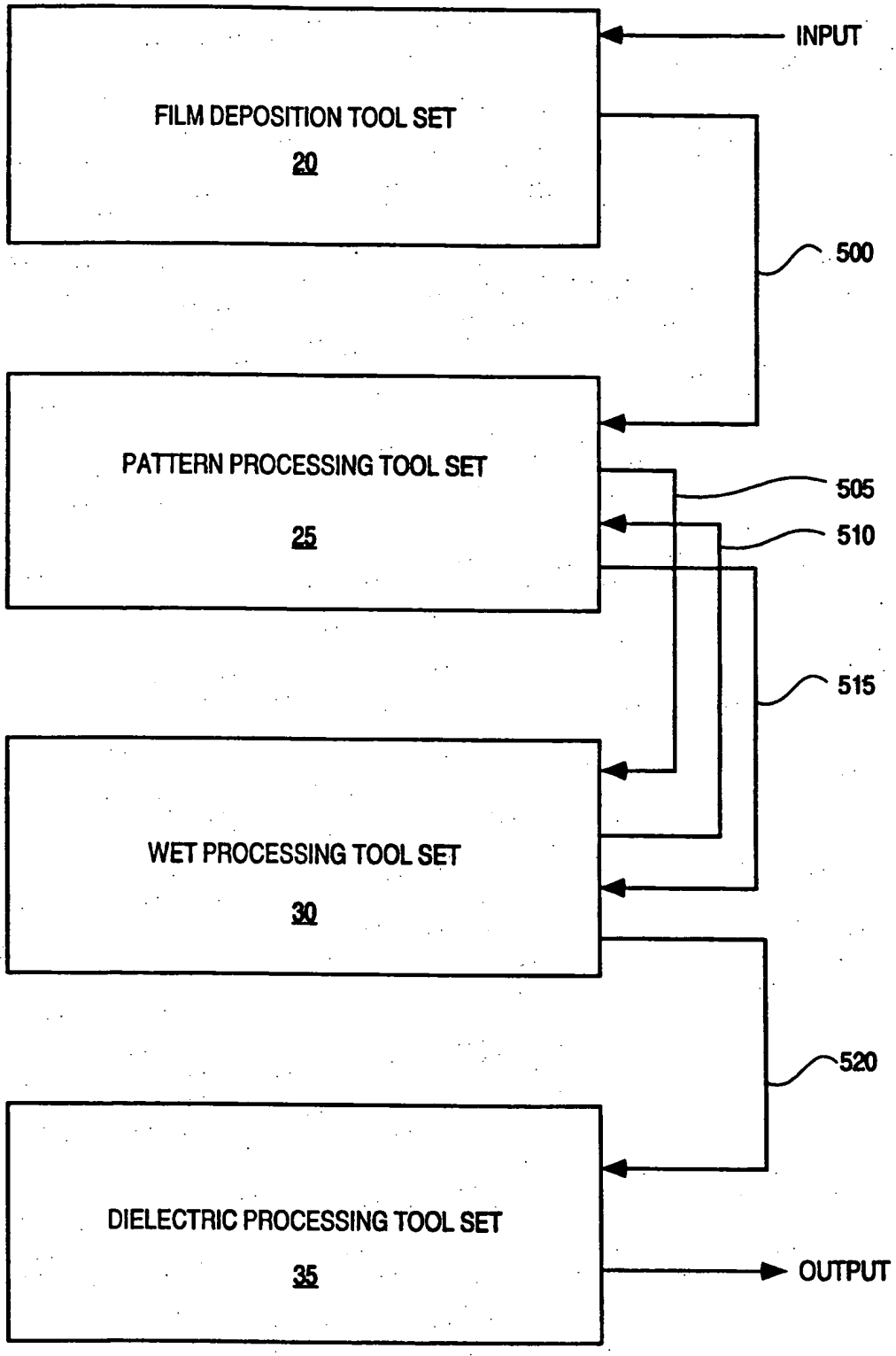

INPUT
FILM DEPOSITION TOOL SET
20
500
PATTERN PROCESSING TOOL SET
25
505
510
515
WET PROCESSING TOOL SET
30
520
DIELECTRIC PROCESSING TOOL SET
35
OUTPUT

FIG. 7

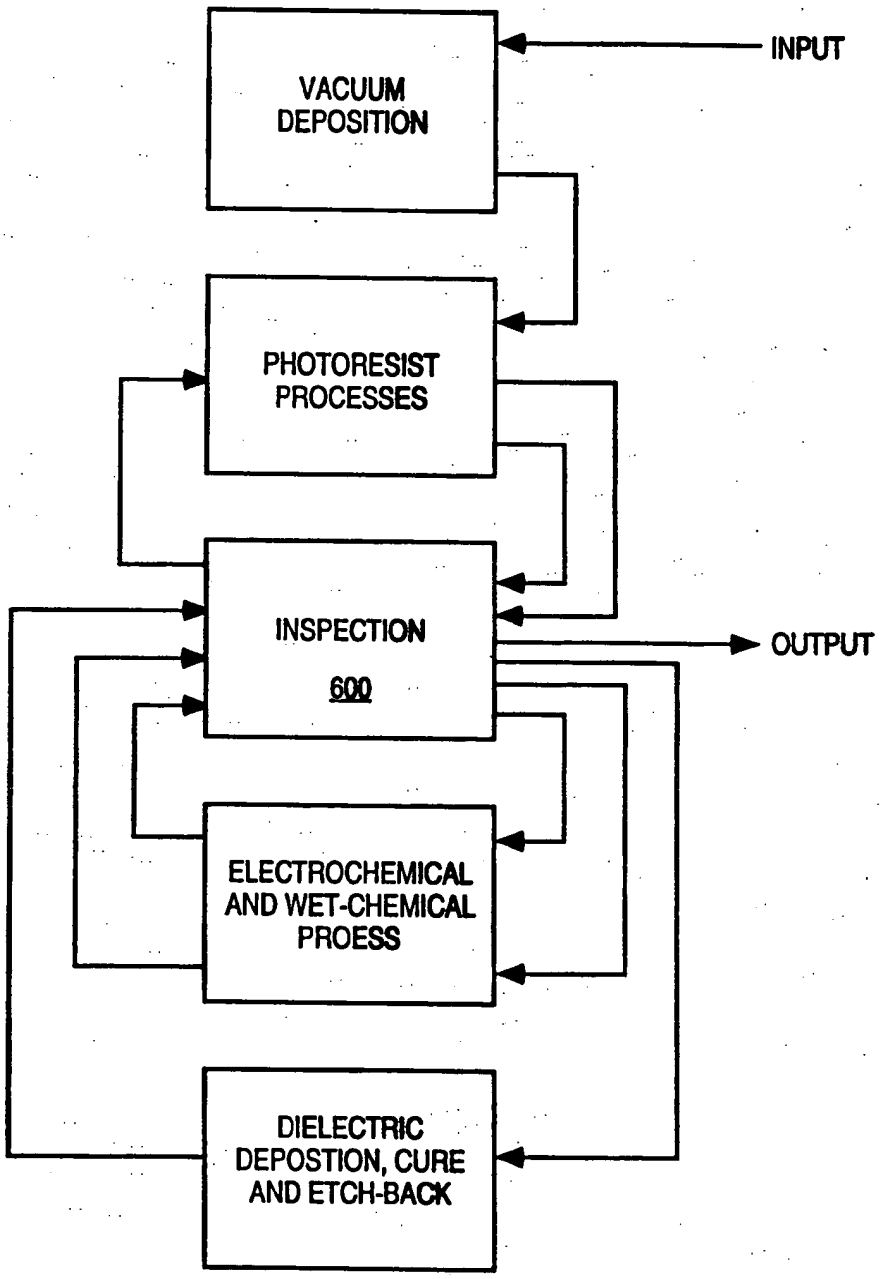

INPUT
VACUUM DEPOSITION
PHOTORESIST PROCESSES
INSPECTION
600
OUTPUT
ELECTROCHEMICAL AND WET-CHEMICAL PROESS
DIELECTRIC DEPOSTION, CURE AND ETCH-BACK

FIG. 8

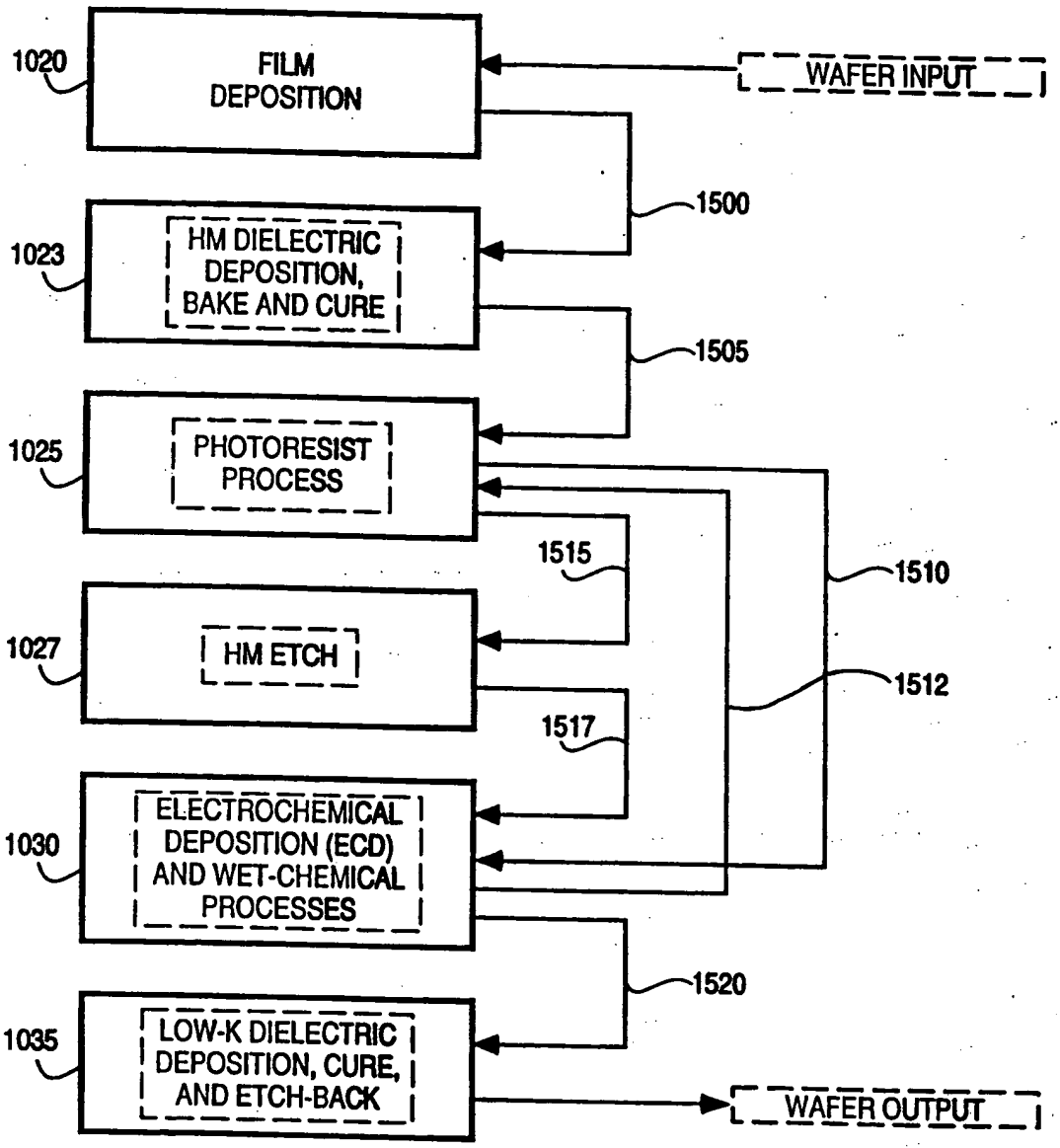

1020
FILM DEPOSITION
WAFER INPUT
1500
1023
HM DIELECTRIC DEPOSITION, BAKE AND CURE
1505
1025
PHOTORESIST PROCESS
1515
1510
1027
HM ETCH
1512
1517
1030
ELECTROCHEMICAL DEPOSITION (ECD) AND WET-CHEMICAL PROCESSES
1520
1035
LOW-K DIELECTRIC DEPOSITION, CURE, AND ETCH-BACK
WAFER OUTPUT

FIG. 9

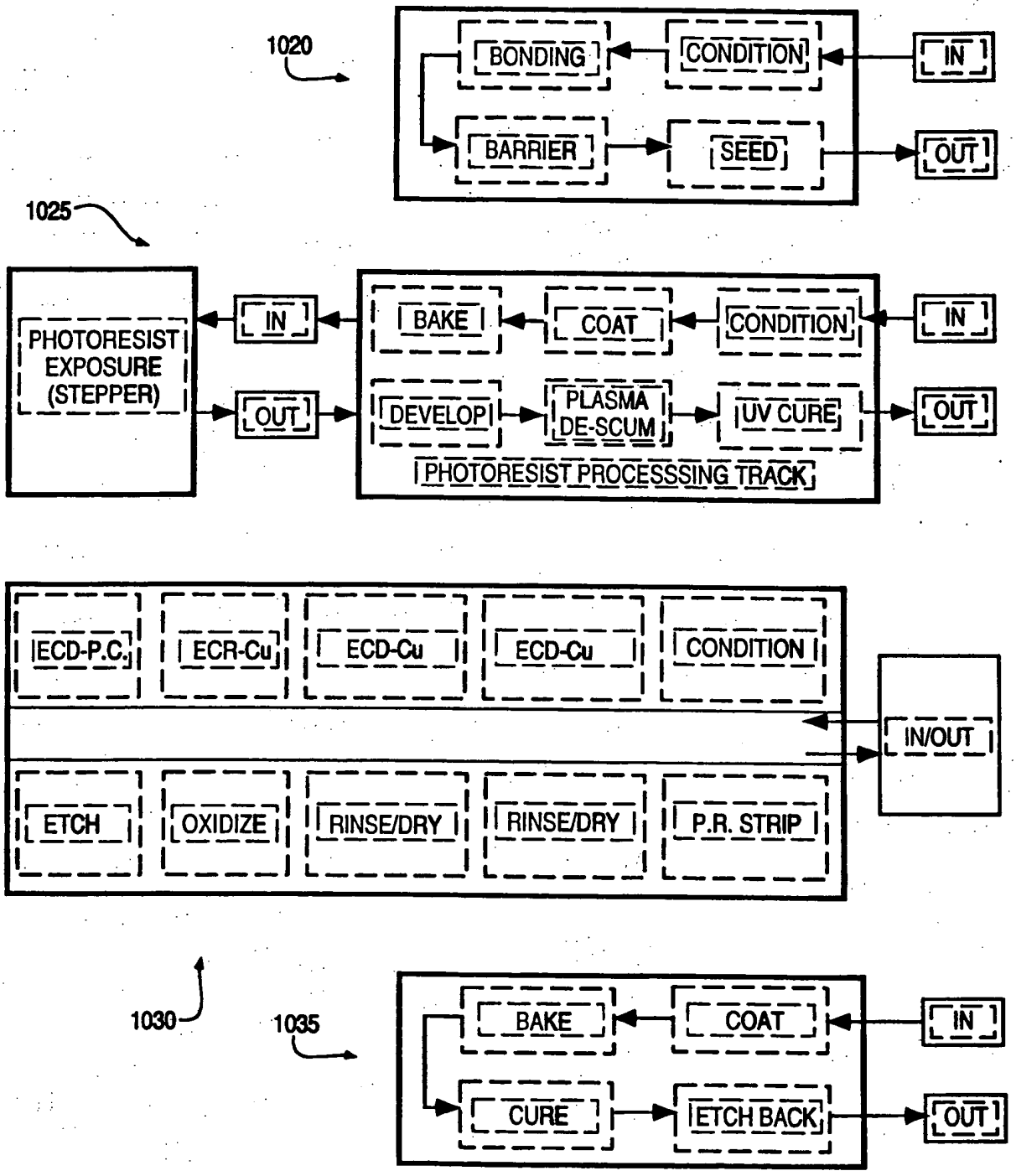

1020
BONDING
CONDITION
IN
BARRIER
SEED
OUT
1025
PHOTORESIST EXPOSURE (STEPPER)
IN
OUT
BAKE
COAT
CONDITION
IN
DEVELOP
PLASMA DE-SCUM
UV CURE
OUT
PHOTORESIST PROCESSSING TRACK
ECD-P.C.
ECR-Cu
ECD-Cu
ECD-Cu
CONDITION
IN/OUT
ETCH
OXIDIZE
RINSE/DRY
RINSE/DRY
P.R. STRIP
1030
1035
BAKE
COAT
IN
CURE
ETCH BACK
OUT

FIG. 10

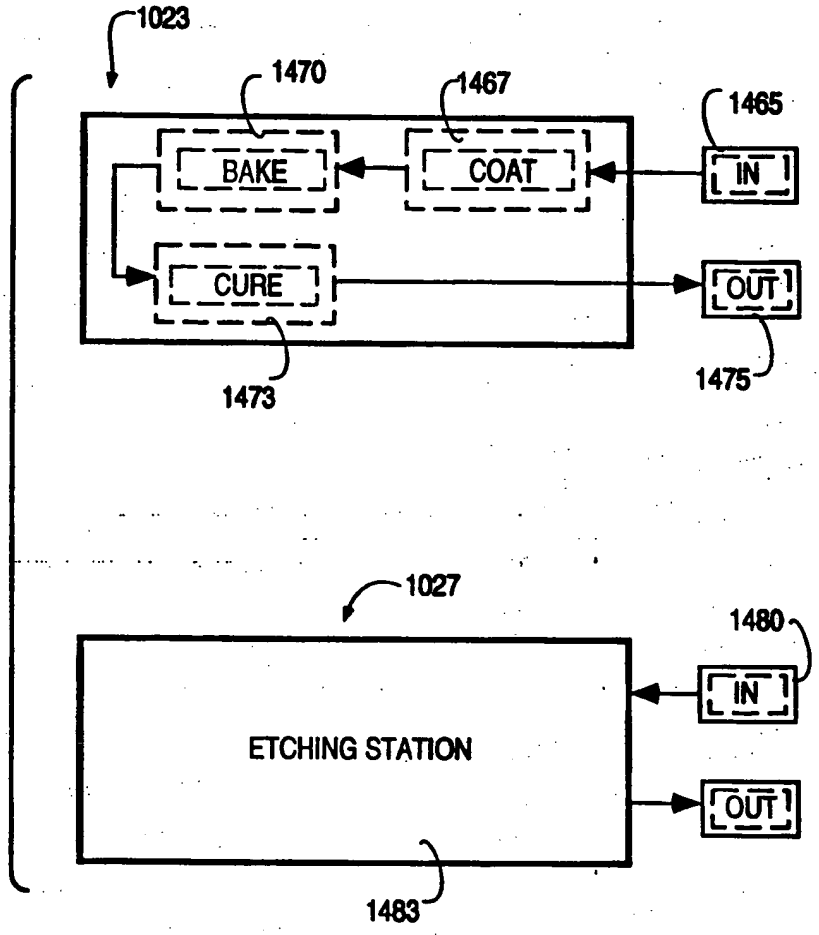

1023
1470
1467
1465
BAKE
COAT
IN
CURE
OUT
1473
1475
1027
1480
IN
ETCHING STATION
OUT
1483

FIG. 11

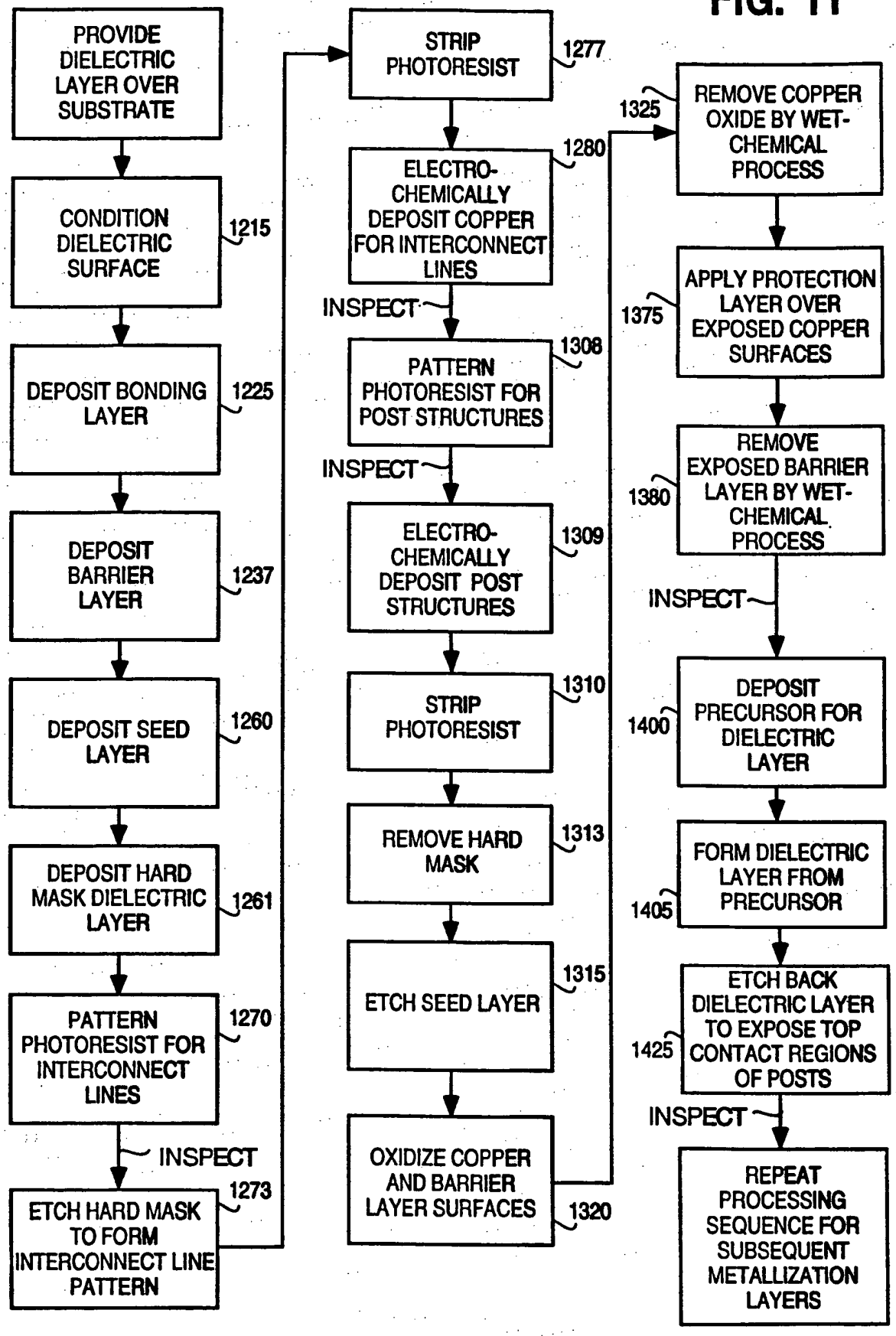

PROVIDE DIELECTRIC LAYER OVER SUBSTRATE
CONDITION DIELECTRIC SURFACE
1215
DEPOSIT BONDING LAYER
1225
DEPOSIT BARRIER LAYER
1237
DEPOSIT SEED LAYER
1260
DEPOSIT HARD MASK DIELECTRIC LAYER
1261
PATTERN PHOTORESIST FOR INTERCONNECT LINES
1270
INSPECT
ETCH HARD MASK TO FORM INTERCONNECT LINE PATTERN
1273
STRIP PHOTORESIST
1277
ELECTRO-CHEMICALLY DEPOSIT COPPER FOR INTERCONNECT LINES
1280
INSPECT
PATTERN PHOTORESIST FOR POST STRUCTURES
1308
INSPECT
ELECTRO-CHEMICALLY DEPOSIT POST STRUCTURES
1309
STRIP PHOTORESIST
1310
REMOVE HARD MASK
1313
ETCH SEED LAYER
1315
OXIDIZE COPPER AND BARRIER LAYER SURFACES
1320
REMOVE COPPER OXIDE BY WET-CHEMICAL PROCESS
1325
APPLY PROTECTION LAYER OVER EXPOSED COPPER SURFACES
1375
REMOVE EXPOSED BARRIER LAYER BY WET-CHEMICAL PROCESS
1380
INSPECT
DEPOSIT PRECURSOR FOR DIELECTRIC LAYER
1400
FORM DIELECTRIC LAYER FROM PRECURSOR
1405
ETCH BACK DIELECTRIC LAYER TO EXPOSE TOP CONTACT REGIONS OF POSTS
1425
INSPECT
REPEAT PROCESSING SEQUENCE FOR SUBSEQUENT METALLIZATION LAYERS

FIG. 12

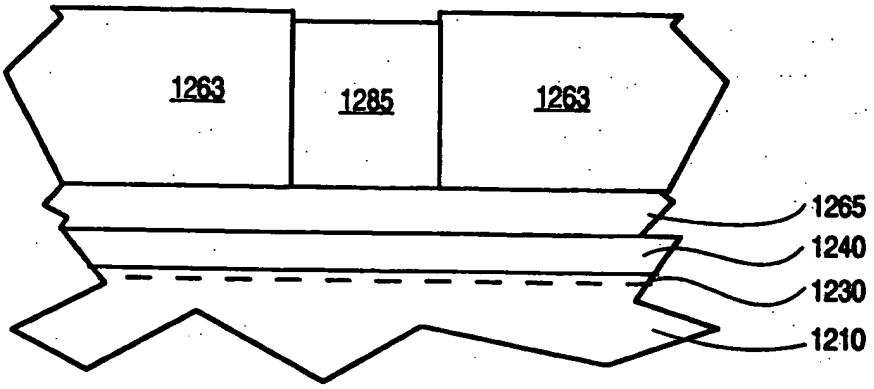


FIG. 13

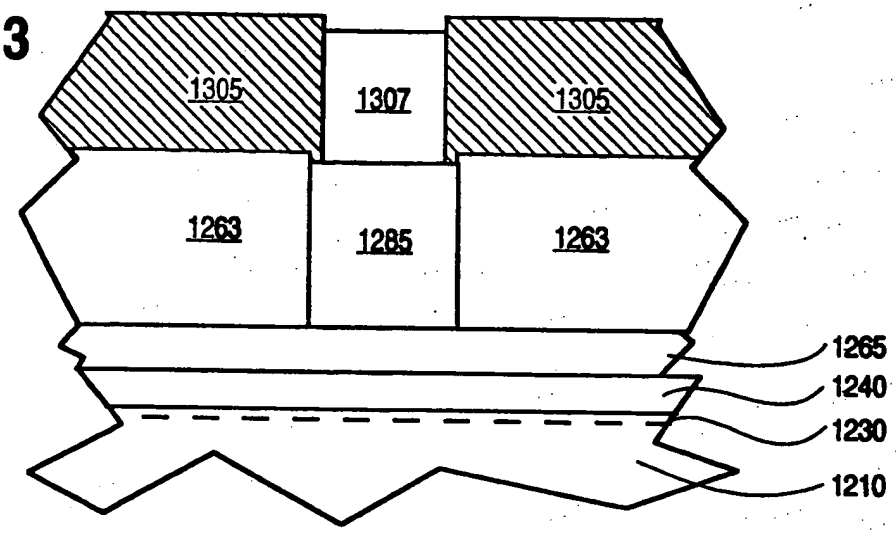


FIG. 14

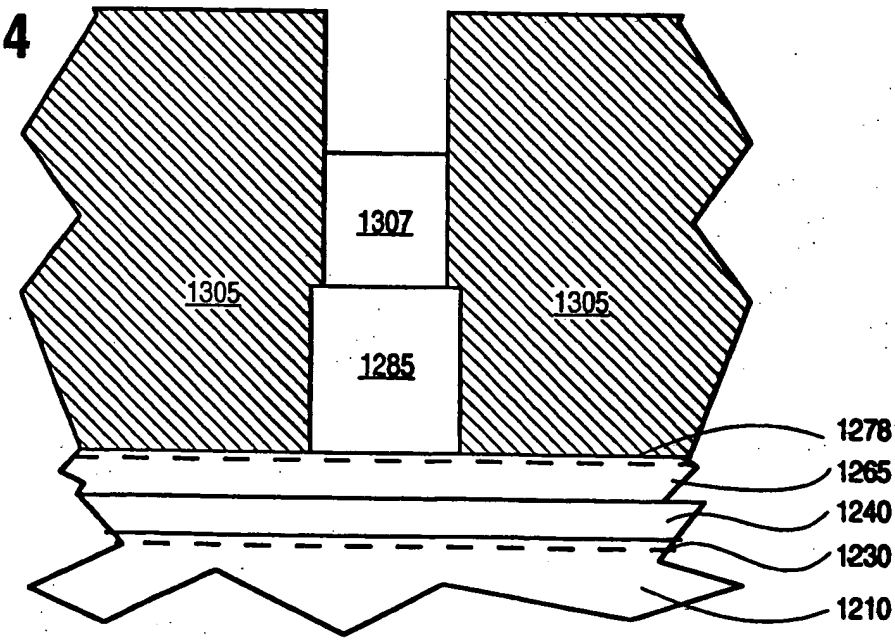


FIG. 15

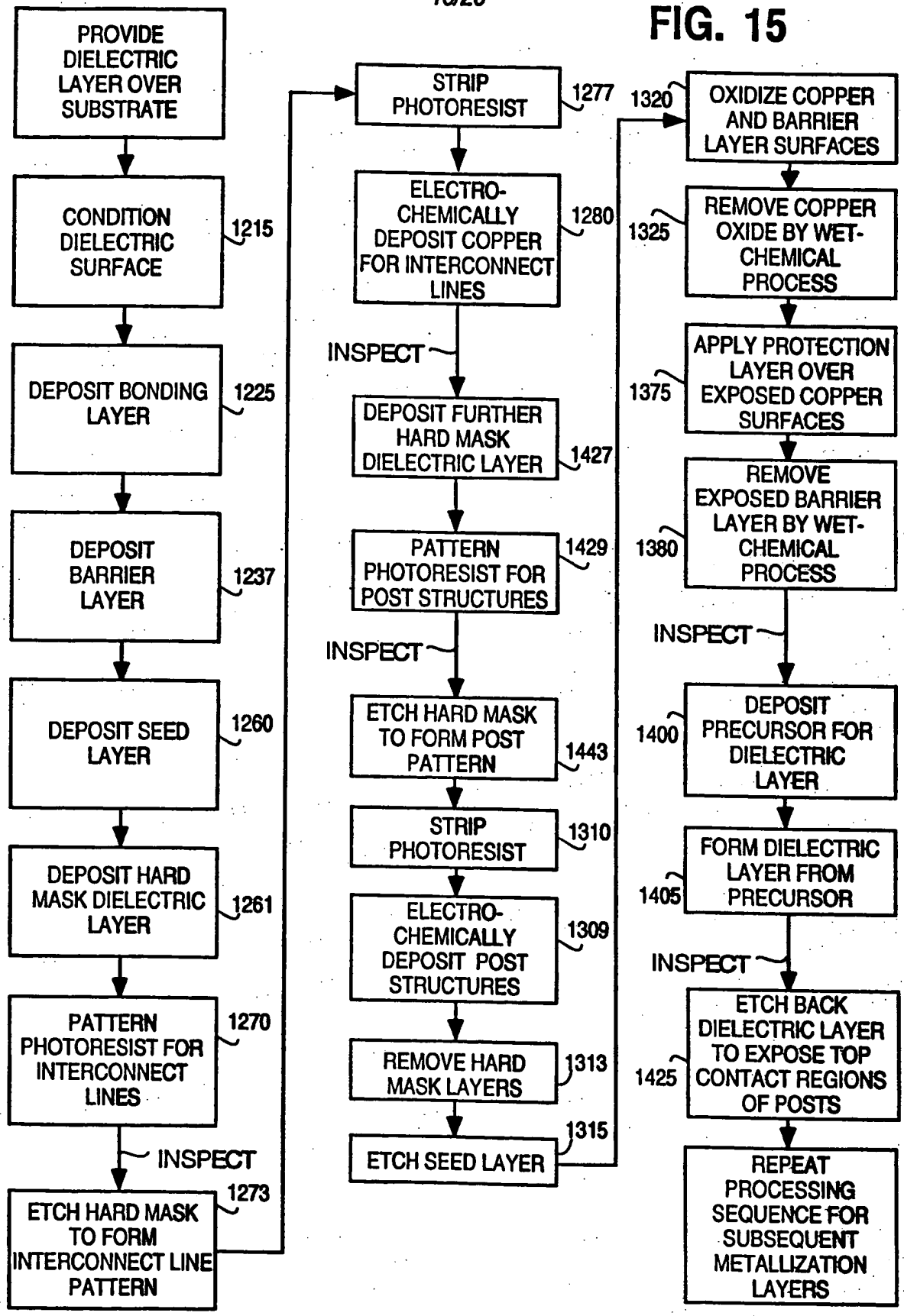

PROVIDE DIELECTRIC LAYER OVER SUBSTRATE
CONDITION DIELECTRIC SURFACE
1215
DEPOSIT BONDING LAYER
1225
DEPOSIT BARRIER LAYER
1237
DEPOSIT SEED LAYER
1260
DEPOSIT HARD MASK DIELECTRIC LAYER
1261
PATTERN PHOTORESIST FOR INTERCONNECT LINES
1270
INSPECT
ETCH HARD MASK TO FORM INTERCONNECT LINE PATTERN
1273
STRIP PHOTORESIST
1277
ELECTRO-CHEMICALLY DEPOSIT COPPER FOR INTERCONNECT LINES
1280
INSPECT
DEPOSIT FURTHER HARD MASK DIELECTRIC LAYER
1427
PATTERN PHOTORESIST FOR POST STRUCTURES
1429
INSPECT
ETCH HARD MASK TO FORM POST PATTERN
1443
STRIP PHOTORESIST
1310
ELECTRO-CHEMICALLY DEPOSIT POST STRUCTURES
1309
REMOVE HARD MASK LAYERS
1313
ETCH SEED LAYER
1315
1320
OXIDIZE COPPER AND BARRIER LAYER SURFACES
1325
REMOVE COPPER OXIDE BY WET-CHEMICAL PROCESS
1375
APPLY PROTECTION LAYER OVER EXPOSED COPPER SURFACES
1380
REMOVE EXPOSED BARRIER LAYER BY WET-CHEMICAL PROCESS
INSPECT
1400
DEPOSIT PRECURSOR FOR DIELECTRIC LAYER
1405
FORM DIELECTRIC LAYER FROM PRECURSOR
INSPECT
1425
ETCH BACK DIELECTRIC LAYER TO EXPOSE TOP CONTACT REGIONS OF POSTS
REPEAT PROCESSING SEQUENCE FOR SUBSEQUENT METALLIZATION LAYERS

FIG. 16

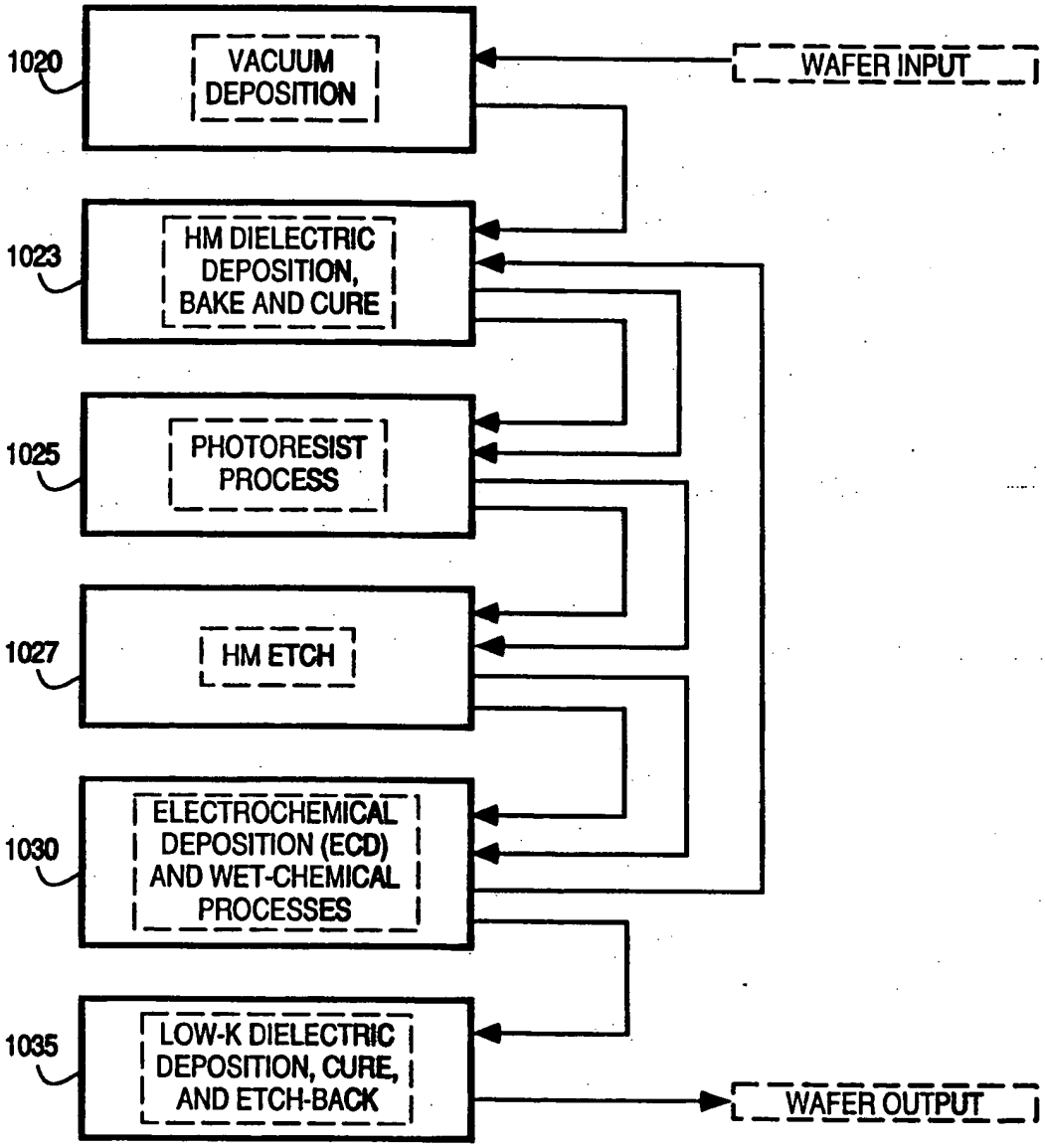

1020
VACUUM DEPOSITION
WAFER INPUT
1023
HM DIELECTRIC DEPOSITION, BAKE AND CURE
1025
PHOTORESIST PROCESS
1027
HM ETCH
1030
ELECTROCHEMICAL DEPOSITION (ECD) AND WET-CHEMICAL PROCESSES
1035
LOW-K DIELECTRIC DEPOSITION, CURE, AND ETCH-BACK
WAFER OUTPUT

FIG. 17

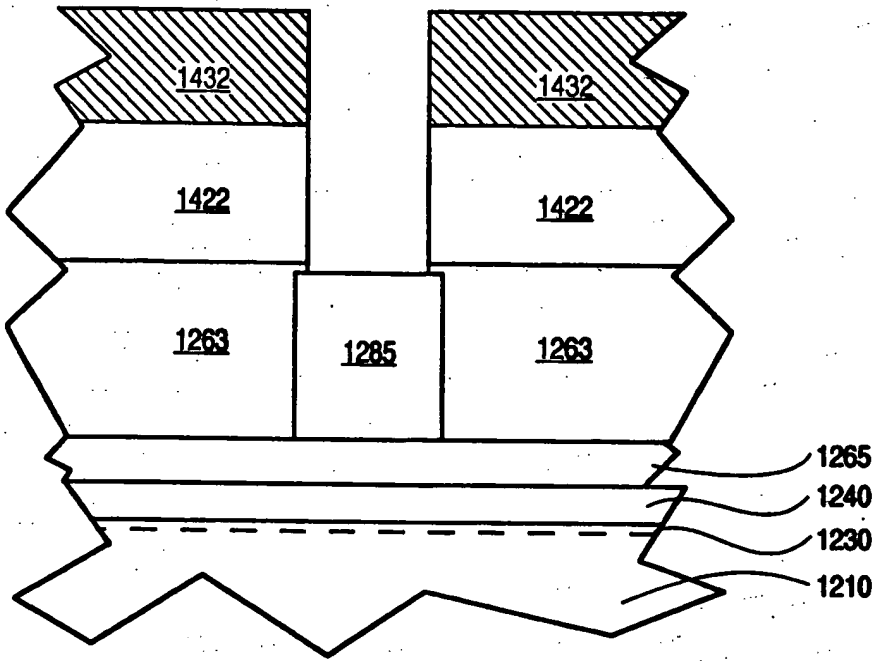

1432
1432
1422
1422
1263
1285
1263
1265
1240
1230
1210

FIG. 18

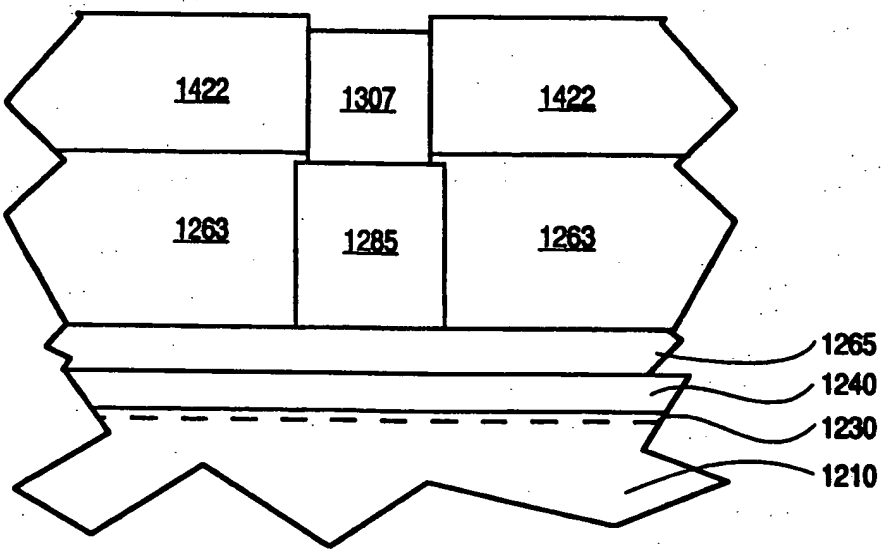

1422
1307
1422
1263
1285
1263
1265
1240
1230
1210

FIG. 19

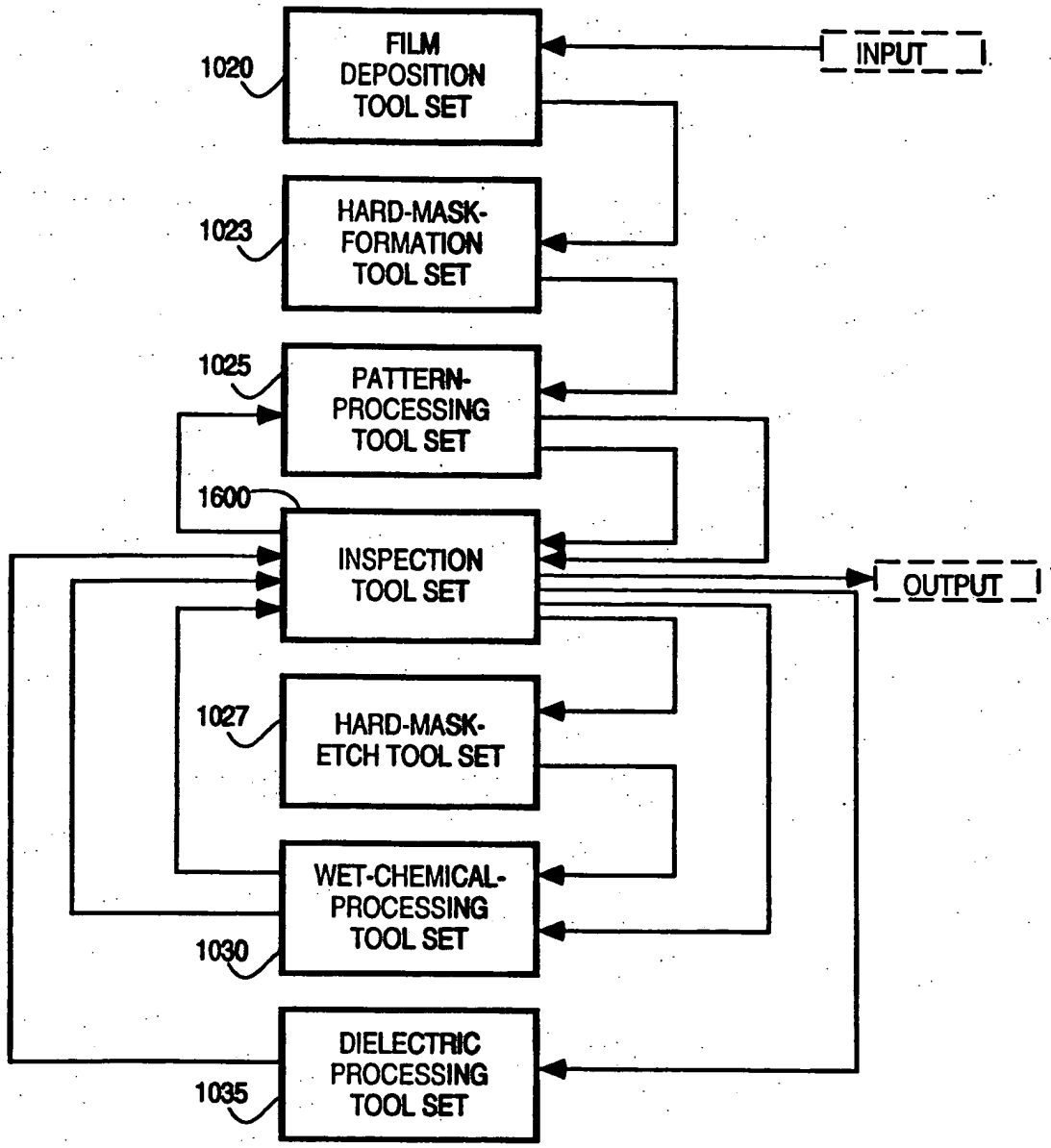
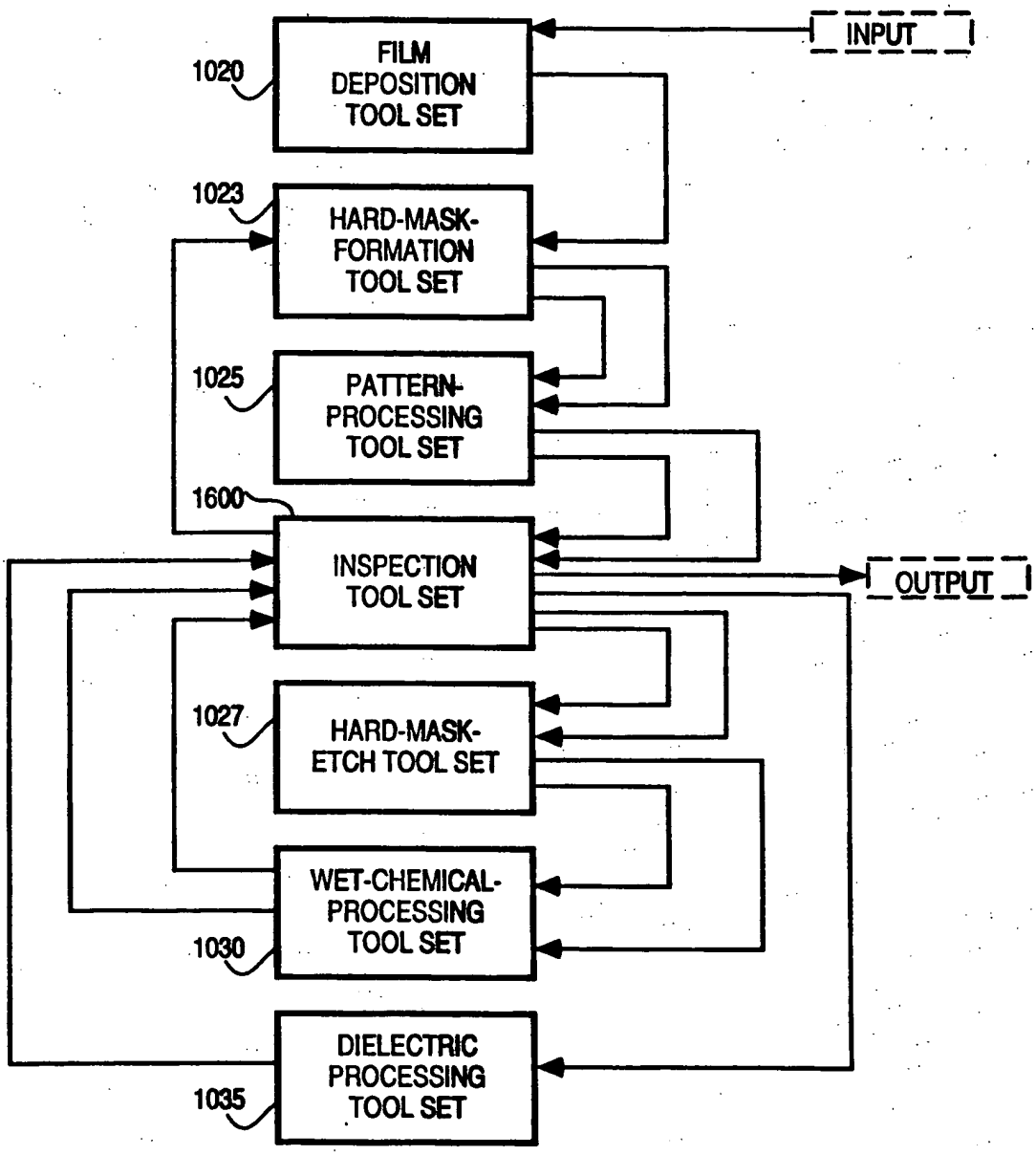

FILM DEPOSITION TOOL SET
1020
INPUT
HARD-MASK-FORMATION TOOL SET
1023
PATTERN-PROCESSING TOOL SET
1025
1600
INSPECTION TOOL SET
OUTPUT
HARD-MASK-ETCH TOOL SET
1027
WET-CHEMICAL-PROCESSING TOOL SET
1030
DIELECTRIC PROCESSING TOOL SET
1035

FIG. 20


INPUT
1020
FILM DEPOSITION TOOL SET
1023
HARD-MASK-FORMATION TOOL SET
1025
PATTERN-PROCESSING TOOL SET
1600
INSPECTION TOOL SET
OUTPUT
1027
HARD-MASK-ETCH TOOL SET
WET-CHEMICAL-PROCESSING TOOL SET
1030
DIELECTRIC PROCESSING TOOL SET
1035

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(71) Applicant: SEMITOOL, INC. [US/US]; 655 West Reserve Drive, Kalispell, MT 59901 (US).

(72) Inventors: STEVENS, E., Henry; 18 Loma Linda Drive, Colorado Springs, CO 80906 (US). BERNER, Robert, W.; 2831 West Timber Drive, Eagle, ID 83616 (US).

(74) Agent: CHAPA, Lawrence, J.; Rockey, Milnamow & Katz, Two Prudential Plaza, 47th floor, 180 North Stetson Avenue, Chicago, IL 60601 (US).

(54) Title: PROCESS AND MANUFACTURING TOOL ARCHITECTURE FOR USE IN THE MANUFACTURE OF ONE OR MORE METALLIZATION LEVELS ON A WORKPIECE

(57) Abstract

A semiconductor manufacturing tool configuration and corresponding process for applying one or more levels of interconnect metallization to a generally planar dielectric surface of a semiconductor workpiece with a minimal number of workpiece transfer operations between the tool sets is disclosed.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/10331

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :Please See Extra Sheet.
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS, USPTO WEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,178,682 A (Tsukamoto et al) 12 January 1993 (12/01/93) col. 17 to 18, lines 13-60 to 1-59	1-66 and 164-198
X	US 5,302,209 A (Maeda et al), 12 April 1994 (12/04/94) col. 11 to 12, lines 24-29 to 1-38	1-66 and 164 to 198
X	US 5,563,095 A (Frey) 08 October 1996 (08/10/96) col. 15 to 16, lines 43-67 and 1-67	1-66 and 164 to 198
X,E	US 5,994,678 A (Zhao et al) 30 November 1999 (30/11/99) col. 41 to 42, lines 29-67 to 1-65	1-66 and 164 to 198

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,E	US 5,933,758 A (Jain) 03 August 1999 (03/05/99) col. 7 to 8, lines 54-67 to 1-32	67-163
X	US 5,256,565 A (Bernhardt et al) 26 October 1993 (26/10/93) col. 6, lines 43-66	67-112, 114-163
Y	US 5,316,974 A (Crank) 31 May 1994 (31/05/94) col. 4, lines 36-62	113

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A. CLASSIFICATION OF SUBJECT MATTER:
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A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

438/634, 644, 645, 685, 687, 692; 118/50.1, 620, 718, 719, 722, 724, 725, 728, 729, 730; 156/345, 643, 646, 656, 657; 219/121.4, 121.42, 121.43

B. FIELDS SEARCHED
Minimum documentation searched
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